Assignment 9

The due date for submitting this assignment has passed.
As our records show you have not submitted this assignment.

1. The first stage of a 5-stage SimpleRISC pipelined processor is -
   - Instruction fetch stage
   - Instruction fetch stage
   - Memory access stage
   - Register write stage
   Accepted/Answered: Instruction fetch stage
   Grade: 0
   1 point

2. The length of the opcode of a pipeline stage instruction consumes -
   - 2 bits
   - 4 bits
   - 5 bits
   - 6 bits
   Accepted/Answered: 5 bits
   Grade: 0
   1 point

3. The value of the immediate in a 3-stage SimpleRISC pipelined processor is compared in the -
   - Instruction fetch stage
   - Instruction fetch stage
   - Memory access stage
   - Register write stage
   Accepted/Answered: Memory access stage
   Grade: 0
   1 point

4. The arithmetic and logical operations in a 5-stage SimpleRISC pipelined processor are executed in the -
   - Control unit
   - ALU
   Accepted/Answered: ALU
   Grade: 0
   1 point

5. Load and store operations in a 5-stage SimpleRISC pipelined processor are executed in the -
   - Instruction fetch stage
   - Instruction fetch stage
   - Memory access stage
   - Register write stage
   Accepted/Answered: Memory access stage
   Grade: 0
   1 point

6. Which of the following elements of the processor is not a part of the data path?
   - Control unit
   - ALU
   - Memory
   Accepted/Answered: Control unit
   Grade: 0
   1 point

7. Which of the following components is used to select between the branch PC and PC+4 value in the IF stage of the pipelined processor?
   - Decoder
   - CRP gates
   - NTR gates
   Multiplier
   Accepted/Answered: Multiplier
   Grade: 0
   1 point

8. The , instruction loads the instruction register (IR) with the contents of the instruction in a microprogrammed processor
   - immword
   - memword
   - instIR
   - immIR
   Accepted/Answered: instIR
   Grade: 0
   1 point

9. The total size of the encoded instruction for horizontal microprogramming is -
   - 60 bits
   - 40 bits
   - 32 bits
   - 10 bits
   Accepted/Answered: 60 bits
   Grade: 0
   1 point

10. Which of the following takes the implementation of instructions in microprogramming header?
    - Implementing complete instructions
    - Pipelining in pipelining architectures
    - Dynamic change in behavior
    - All of the above
    Accepted/Answered: All of the above
    Grade: 0
    1 point

Due on 2020-04-01, 23:59 IST.