

Unit 7 - Week 6

Course outline

How does an NPTEL online course work?

Week 1

Week 2

Week 3

Week 4

Week 5

Week 6

Translation Lookaside Buffer, Large Pages, Boot Sector

Loading the kernel, Initializing the Page table

Setting up page tables for user processes

Quiz : Assignment 6

Week 6 Feedback Form

Week 7

Week 8

Week 9

Week 10

Week 11

Week 12

Assignment Solution

Download Videos

Text Transcripts

Assignment 6

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2020-03-11, 23:59 IST.

1) Consider a paging hardware with a TLB. Assume that the entire page table and all the pages are in the physical memory. It takes 10 milliseconds to search the TLB and 80 milliseconds to access the physical memory. If the TLB hit ratio is 0.6, the effective memory access time (in milliseconds) is _____.

No, the answer is incorrect.
Score: 0

Accepted Answers:
(Type: Numeric) 122

3 points

2) If an instruction takes i microseconds and a page fault takes an additional j microseconds, the effective instruction time if on the average a page fault **1 point** occurs every k instruction is-

$i+j/k$

$i+j \times k$

$(i+j)/k$

$(i+j) \times k$

No, the answer is incorrect.
Score: 0

Accepted Answers:
 $i+j/k$

3) Consider a three level paging scheme with a TLB. Assume no page fault occurs. It takes 20 ns to search the TLB and 100 ns to access the physical **3 points** memory. If TLB hit ratio is 80%, the effective memory access time is _____ msec.

180 ns

120 ns

40ns

80ns

No, the answer is incorrect.
Score: 0

Accepted Answers:
180 ns

4) Which of the following is true: **1 point**

TLBs have hit ratio of 99+ percent

TLBs are generally located on the same chip as processor

TLBs are fully-associative

All of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
All of the above

5) What is the size of a Sector on the disk: **1 point**

4MB

4KB

512B

4B

No, the answer is incorrect.
Score: 0

Accepted Answers:
512B

6) Which of the following can be seen as effect of using Large pages: **1 point**

There will be decrease in number of elements in the TLB required to maintain the same hit ratio

The kernel is required to manage the cases of segmentation

Single layer of paging table required

The kernel has to ensure that the large process are assigned large pages and they are using it efficiently.

All of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
All of the above