Assignment 6

The due date for submitting this assignment has passed. As per our records you have not submitted this assignment.

1) Consider a paging hardware with a TLB. Assume that the entire page table and all the pages are in the physical memory. It takes 10 milliseconds to search the TLB and 80 milliseconds to access the physical memory. If the TLB hit ratio is 0.6, the effective memory access time (in milliseconds) is ________.

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 122

2) If an instruction takes 1 microsecond and a page fault takes an additional 1 microsecond, the effective instruction time if on the average a page fault occurs every k instructions is:

- 1 + jk
- 1 + jk
- 1 + jk
- 1 + jk

No, the answer is incorrect.
Score: 0
Accepted Answers:
13k

3) Consider a three level paging scheme with a TLB. Assume no page fault occurs. It takes 20 ns to search the TLB and 100 ns to access the physical memory. If TLB hit ratio is 90%, the effective memory access time is ________.

- 180 ns
- 120 ns
- 40 ns
- 80 ns

No, the answer is incorrect.
Score: 0
Accepted Answers:
180 ns

4) Which of the following is true:

- TLBs have hit ratio of 98+ percent
- TLBs are generally located on the same chip as processor
- TLBs are fully-associative
- All of the above

No, the answer is incorrect.
Score: 0
Accepted Answers:
All of the above

5) What is the size of a Sector on the disk:

- 4MB
- 4KB
- 512B
- 4B

No, the answer is incorrect.
Score: 0
Accepted Answers:
512B

6) Which of the following can be seen as effect of using Large pages:

- There will be decrease in number of elements in the TLB required to maintain the same hit ratio
- The kernel is required to manage the cases of segmentation
- Single layer of paging table required
- The kernel has to ensure that the large process are assigned large pages and they are using it efficiently.
- All of the above

No, the answer is incorrect.
Score: 0
Accepted Answers:
All of the above