Digital System design with PLDs and FPGAs

Module 1: Problem

An FSM has three inputs. First one is an input pulse of duration 10 ns occurring every 1 us, where the detection of it doesn’t have any critical timing constraint, second input is a pulse which has to detected within 40 ns of its occurrence, third is a pulse from the decoder of a counter working at 20 MHz indicating counter has reached a particular count, to be detected by FSM. Estimate the minimum frequency of the clock to FSM?