Digital System design with PLDs and FPGAs

Module 2: Problem

Given below is a VHDL code in dataflow model with concurrent statements. Rewrite the VHDL code concisely using behavioral code with minimum number of processes for the same functionality.

```vhdl
library ieee; use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all; use ieee.std_logic_arith.all;

entity mod1 is
  port (a, b, c: in std_logic_vector (2 downto 0);
        p, q, r: in std_logic_vector (3 downto 0);
        x, y, z: out std_logic_vector (2 downto 0));
end mod1;

architecture dflow of mod1 is
begin
  x <= b when (p <= q) else
      b when (r > 2) else
      c;
  y <= a when (p > q) else
      b when (r = 3) else
      c;
  z <= c when (p > q) else
      b;
end dflow;
```