15 Week Lecture Plan:

Week	Unit / Hours	Lecture topics	Lab Topics
Week – 1	Unit – 1 (2.5 Hours)	MOS Transistor – Detailed Study	CMOS Concepts HSPICE Simulations
Week – 2	Unit – 2 (2.5 Hours)	Combinational Circuits & Layout, Delay, Sequential Circuits	Layout Design Delay Estimation Layout Comparison
Week – 3	Unit – 2 (2.5 Hours)	Logical Effort and Circuit Families	Logic Effort Design Optimization HSPICE Simulations
Week – 4	Unit – 3 (3 Hours)	Introduction to Synthesis, Libraries	Basic Concepts of Synthesis Libraries
Week – 5	Unit – 3 (3 Hours)	RTL Coding for Synthesis , Reading design in DC, Design Environment	Simulation, Synthesis Mismatch Library setting and Parsing the design
Week – 6	Unit – 3 (3 Hours)	Design Constraints , Compile Flow & Strategies, DC_Lab-1	Environment Setup Design constraints
Week – 7	Unit – 3 (2 Hours)	DC_Lab-2, DC_Lab-3	Compile flow strategies Library Setting and Parsing the design
Week – 8	Unit – 3 (2.5 Hours)	Analysis & Reporting, DC_Lab-4	Define constraints Compiling the design Analysis of reports
Week – 9	Unit – 4 (2 Hours)	Advance Synthesis Techniques - 1 & 2	Advanced Synthesis Optimization techniques
Week – 10	Unit – 4 (3 Hours)	Power Methodology and Analysis, DC_Lab-5	Power Analysis
Week – 11	Unit – 5 (3 Hours)	STA – Concepts & Flow, Interconnects and Delay Calculation, Clocks and Exceptions	Static Timing analysis
Week – 12	Unit – 5 (3.5 Hours)	PT_Lab-1, On-Chip variation, Cross talk and noise	Interconnects and delay calculation
Week – 13	Unit – 5 (2.5 Hours)	Introduction to Process Variation, SSTA, Equivalence Checking/Formality	Clocks and Exceptions Maximum Load
Week – 14	Unit – 5 (2.5 Hours)	PT_Lab-2 and PT_Lab-3	STA What if analysis
Week – 15	Unit – 5 (1.5 Hours)	DC_Lab-6, Summary and Project	Bottom up compile with charecterization

40 hour lecture plan

Hour	Lecture Name	Learning Outcomes Mapping
Hour – 1	MOS Transistor	L1
Hour - 2.5	MOS Transistor - Detailed Study	L1
Hour - 3.5	Combinational Circuits & Layout	L1
Hour - 4.5	Delay	L1
Hour - 5.5	Sequential Circuits	L1
Hour - 6.5	Logical Effort	L2
Hour - 7.5	Circuit Families	L1
Hour - 8.5	Introduction to Synthesis	L2
Hour - 10.5	Libraries	L2
Hour - 11.5	RTL Coding For Synthesis	L2
Hour - 12.5	Reading Design in DC	L3
Hour - 13.5	Design Environment	L3
Hour - 14.5	Design Constraints	L3
Hour - 15.5	Compile Flow & Strategies	L3
Hour - 16.5	DC Lab_1	L2
Hour - 17.5	DC Lab_2	L3
Hour - 18.5	DC Lab_3	L3
Hour - 19.5	Analysis & Reporting	L3
Hour - 21	DC Lab_4	L3
Hour - 22	Advanced Synthesis Techniques - 1	L4
Hour - 23	Advanced Synthesis Techniques - 2	L4
Hour - 25	Power Methodology and Analysis	L5
Hour - 26	DC Lab_5	L5
Hour - 27.5	Static Timing Analysis - Concepts & Flow	L6
Hour - 28.5	Interconnects And Delay Calculation	L6
Hour - 30	Clocks And Exceptions	L6
Hour - 31.5	PT Lab_1	L6
Hour - 32.5	On Chip Variation	L6
Hour - 33.5	Cross Talk And Noise	L6
Hour - 34.5	Introduction to Process Variation, SSTA	L6
Hour - 36	Equivalence Checking/Formality	L6
Hour - 37.5	PT Lab_2	L6
Hour - 38.5	PT Lab_3	L6
Hour - 39.5	DC Lab_6	L6
Hour - 40	Summary & Project	L2,L3,L4,L5,L6