

Advanced Logic Synthesis

Multiple Choice Questions

1. State whether the following statement is either True or False. Pure silicon has no free carriers and conducts poorly.
 - a. True
 - b. False
2. From the following options, how will you increase the conductivity of pure silicon?
 - a. Doping Group -V Elements
 - b. Doping Group – III elements
 - c. Both a and b
 - d. None of the above
3. What happens when NMOS gate is at a low voltage?
 - a. P-Type body is at low voltage
 - b. Source-body and drain-body diodes are off
 - c. No current flows, transistor is off
 - d. All of the above
4. The voltage at the gate on NMOS is _____ when there is a positive charge on gate of the MOS capacitor and transistor is ON.
 - a. High
 - b. Low
5. In layout designing, Feature Size F represents?
 - a. The distance between Source and Drain, set by minimum width of Polysilicon
 - b. The distance between Gate and Source, set by minimum width of Polysilicon
 - c. The distance between Gate and Drain, set by minimum width of Polysilicon
 - d. None of the above
6. What are the characteristics of NMOS transistor in the cut-off region?
 - a. Negative voltage on the Gate attracts holes in substrate towards oxide
 - b. Electrons are pushed deeper into the substrate
 - c. Both a and b
 - d. None of the above
7. When current flows from the drain to source and if I_{ds} increases with V_{ds} , then the transistor would be in _____ region.
 - a. Cut-Off
 - b. Saturation
 - c. Active
 - d. Linear

8. In the Linear region, I_{ds} depends on:
- Charge in the channel
 - Applied voltage
 - How fast is the charge moving
 - Both a and c**
9. Threshold voltage V_t , is a function of _____.
- Gate Material and Gate Insulator thickness
 - Voltage between source and substrate
 - Channel Doping
 - All of the above**
10. If V_t increases, then the _____.
- Current I_{ds} decreases and speed of operation will be slower**
 - Current I_{ds} increases and speed of operation will be higher
 - Current I_{ds} decreases and speed of operation will be higher
 - Current I_{ds} increases and speed of operation will be slower
11. Estimate the delay of a fan-out of 1 inverter using RC delay model
- 8RC
 - 6RC**
 - 4RC
 - 2RC
12. How many transistors are required to design the following equation: $Y = SD1 + SD0$?
- 15
 - 10
 - 20**
 - 5
13. If the width of a transistor increases, the current _____ and its gate capacitance _____:
- Increases and Increases**
 - Decreases and Increases
 - Increases and Decreases
 - Decreases and Decreases
14. If the length of a transistor increases, the current _____ and its gate capacitance _____:
- Increases and Increases
 - Decreases and Increases**
 - Increases and Decreases
 - Decreases and Decreases

15. If the supply voltage of a chip increases, the maximum transistor current_____.
- Increases
 - Decreases
 - Does not change
 - Causes an exponential decay
16. If the supply voltage of a chip increases, the gate capacitance of each transistor_____.
- Increases
 - Decreases
 - Causes an exponential increase
 - Does not change
17. For an NMOS operation, one of the following points are true:
- In Cut-off, $V_{in} < V_{tn}$ – In Linear, $V_{in} > V_{tn}$ and In Saturated, $V_{out} > V_{in} - V_{tn}$
 - In Cut-off, $V_{tn} > V_{in} - V_{tn}$ – In Linear, $V_{in} > V_{tn}$ and In Saturated, $V_{out} > V_{in} - V_{tn}$
 - In Cut-off, $V_{in} < V_{tn}$ – In Linear, $V_{in} > V_{tn}$ and In Saturated, $V_{out} < V_{in} - V_{tn}$
 - In Cut-off, $V_{in} < V_{tn}$ – In Linear, $V_{in} < V_{tn}$ and In Saturated, $V_{out} > V_{in} - V_{tn}$
18. Estimate rising and falling propagation delays of a 2-input NAND driving 'h' identical gates using Elmore Delay
- Rising = $(6 + 4h)RC$ Falling = $(7 + 4h)RC$
 - Rising = $(6 + 4h)RC$ Falling = $(6 + 4h)RC$
 - Rising = $(7 + 4h)RC$ Falling = $(7 + 4h)RC$
 - Cannot be determined
19. In a flip-flop based system, one of the following options is correct.
- Data launches on one rising edge
 - Must setup before next rising edge
 - If data arrives late, System fails; and if data arrives early, time is wasted
 - All of the above
20. In a latch based system, one of the following options is correct.
- Data can pass through latch while transparent
 - Long cycle of logic can borrow time into next
 - Both a and b
 - None of the above
21. State whether the following statement is either True or False. If setup times are violated, you need to increase the clock speed.
- True
 - False
22. State whether the following statement is either True or False. If hold times are violated, chip fails at any speed.
- True
 - False

23. Logical effort is a method to make the following decisions:
- Uses a simple model of delay and allows 'back-of-the envelope' calculations
 - Helps making rapid comparisons between alternatives
 - Emphasizes remarkable symmetries
 - All of the above
24. Delay has 2 components, $d = f + p$, f and p stands for?
- f – Effort Delay and p - Parasitic Delay
 - f – Gate Delay and p – propogational Delay
 - f – Fall Delay and p - propogational Delay
 - None of the above
25. State whether the following statement is either True or False. In a CMOS level implementation, the number of transistors required to build a Nand gate is larger than that of and gate
- True
 - False
26. State whether the following statement is either True or False. Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current
- True
 - False
27. Estimate the frequency of an N-stage ring oscillator with $g = 1$, $h = 1$, $p = 1$ and $d = 2$
- $1/2N$
 - $1/4N$
 - $1/6N$
 - $1/8N$
28. Minimum delay of N stage path is:
- $D = NF \text{ powerof}(1/N) + P$
 - $D = NF \text{ powerof}(N) + P$
 - $D = NF + p$
 - None of the above
29. The group of primitive cells which are used to build larger circuits is called:
- Standard Cells
 - Dummy cells
 - Macro cells
 - None of the above
30. In Logic Synthesis, Translation refers to:

- a. HDL Syntax/Rule Checks
 - b. Converts HDL to functional Boolean equivalent
 - c. Both a and b
 - d. Converts HDL to technology dependent netlist
31. In Logic Synthesis, Mapping and Optimization refers to:
- a. Mapping Boolean equations to technology specific primitive functions
 - b. Modifies mapping to meet design goals
 - c. Mapping Boolean equations to GTECH cells
 - d. Both a and b
32. What are the various factors that need to be considered while choosing a technology library for a design?
- a. PVT conditions
 - b. Technology to which the design has to be mapped
 - c. Wire Load Model
 - d. All of the above
33. When delays are small, power consumption is:
- a. High
 - b. Low
 - c. Cannot be determined
 - d. Does not change
34. Switching point voltage of a cell refers to :
- a. Point on VTC where $V_{Out} = V_{in}$
 - b. Voltage at nominal condition
 - c. Voltage at cutoff condition
 - d. Voltage in triode condition
35. _____ is the current that is consumed when the output is high.
- a. Dynamic leakage current
 - b. Static leakage current
36. The time it takes a driving pin to make a transition from $K(V_{DD})$ to $(1-K)V_{DD}$ value is:
- a. Propagation delay
 - b. Rise transition time
 - c. Fall transition time
 - d. Settling time
37. The time it takes a driving pin to make a transition from $(1-K)V_{DD}$ to $K.V_{DD}$ value is:
- a. Fall Transition Time
 - b. Rise Transition Time

- c. Propagation delay
 - d. Transient time
38. The time difference between the input signal crossing a 0.5VDD and the output signal crossing its 0.5 VDD when the output signal is changing from low to high is:
- a. Propagation Delay low-to-high (Rise Propagation)
 - b. Fall Transition Time
 - c. Rise Transition Time
 - d. Propagation delay low-to-high (Fall Propagation)
39. Switching Fall Power, $P_{swf} =$ _____
- a. $(C_{load} + C_{outf}) * V_{dd} / 2$
40. The time interval during which the clock signal is high or low, so that it ensures proper operation of a flop or a latch is: _____
- a. Clock Pulse Width
41. In a standard cell library, cell logic model is generated by _____.
- a. Characterization Process
42. Characterization computes cell parameters like delay, output current etc. by depending on the following variables.
- a. Output Load
 - b. Input Slew
 - c. Both a and b
 - d. Cannot be computed
43. Advanced optimization strategies include:
- a. Aggressive logic duplication
 - b. Improved technology mapping
 - c. Both a and b
 - d. None of the above
44. Register re-timing works by:
- a. Moving registers through the cones of logic where end-to-end functionality of the circuit is unchanged
 - b. Splitting of merging registers through the cones of logic where end-to-end functionality of the circuit is unchanged
 - c. Merging registers through the cones of logic where end-to-end functionality of the circuit is unchanged
 - d. Moving, Splitting of merging registers through the cones of logic where end-to-end functionality of the circuit is unchanged
45. The largest percentage of static power results from source-to-drain Subthreshold leakage. This is caused by _____.
- a. Reduced threshold voltages that prevent the gate from completely turning off
 - b. Increased threshold voltages that prevent the gate from completely turning off
 - c. Reduced threshold voltages that prevent the gate from completely turning on

Comment [H1]: Please note that there are no options for questions 39, 40 and 41. Please check.

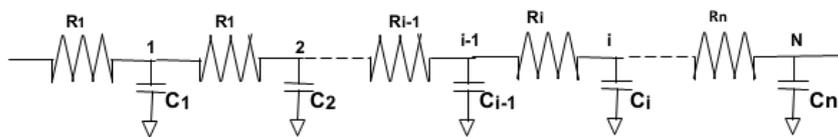
- d. Increased threshold voltages that prevent the gate from completely turning on
46. When transistors switch, both NMOS and PMOS networks may be momentarily ON at one, which leads to:
- Short Circuit current
 - GIDL current
 - DIBL current
 - None of the above
47. In STA, delay is a function of:
- Slew_in, load, P, V, T
 - P, V, T
 - Slew_in and load
 - None of the above
48. Cell delay is generally a function of _____.
- Input transition and output load
 - Input delay and output delay
 - Input capacitance and output transition
 - Input load and output load
49. Which points are true for Pre-Layout STA
- i) No information about the netsii) Estimated net delaysiii) Back annotated net informationiv) Clock network fully implemented
- i), iii), and iv)
 - i) and ii)
 - i), ii), and iii)
 - iii) and iv)
50. Which points are true for Post-Layout STA
- i) No information about the netsii) Estimated net delaysiii) Back annotated net informationiv) Clock network fully implemented
- i), iii), and iv)
 - i) and ii)
 - i), ii), and iii)
 - iii) and iv)
51. In delay calculations, Gate delays are taken from _____ and Net delays are taken from _____
- Libraries, Post layout data
 - Post layout data, Libraries
 - PVT, Wire load
 - Wire load, PVT
52. State whether the following statement is either True or False. Net delay is the total time which needs to charge or discharge all parasitic capacitances of a given net.
- True

- b. False
53. For an edge-triggered element, the time interval before the active clock edge during which the data should be unchanged is called _____.
- Hold Time
 - Skew
 - Setup Time
 - Latency
54. Which of the following points are true for a setup check:
- $T_{pd} + T_{comb} < T_{cp} - T_s$
 - Total data path delay = $T_{pd} + T_{comb}$
 - Setup check limits the data path to a maximum value
 - All of the above
55. Arrival time defines:
- The time interval during which a data signal can arrive at a pin in relation to the nearest edge of the clock signal that triggers the data transition
 - The time interval during which a data signal can arrive at a pin in relation to the last edge of the clock signal that triggers the data transition
 - The time interval during which a data signal can arrive at a pin in relation to the nearest edge of the clock signal that will not trigger the data transition
 - The time interval during which a data signal can arrive at a pin in relation to the last edge of the clock signal that will not trigger the data transition
56. State whether the following statement is either True or False. Pulse width is the time between the active and inactive states of the same signal.
- True
 - False
57. The time available between the asynchronous signal going to inactive to the active clock edge is _____ and the time between active clock edge and asynchronous signal going inactive is _____.
- Recovery Time, Removal Time
 - Setup Time, Hold Time
 - Removal Time, Recovery Time
 - Hold Time, Setup Time
58. Which points are true for a "Net":
- It can travel on multiple metal layers of the chip
 - It is a wire connecting pins of standard cells and blocks
 - It can be broken up into segments for equivalent electrical representation
 - All of the above
59. Interconnect resistance refers to:
- Resistance between the output pin of a cell and the input pins of the fan-out cells

- b. Resistance between the output pin of a cell and the output pins of the fan-out cells
 - c. Resistance between the input pin of a cell and the output pins of the fan-out cells
 - d. None of the above
60. Wireload models are used to estimate:
- a. Resistance and Capacitance
 - b. Area overhead due to interconnect
 - c. Length of the net based on number of fan-outs
 - d. All of the above
61. In the best case interconnect tree, it is assumed that the load pin is physically adjacent to the driver. Thus:
- a. None of the wire resistance is in the path to the destination pin
 - b. All of the wire capacitance and the pin capacitances from other fan-out pins still act as load on the driver pin.
 - c. Both a and b
 - d. None of the above
62. What are the different formats that Parasitics are extracted from a layout:
- a. DSPF
 - b. SPEF
 - c. Both a and b
 - d. None of the above
63. How will you reduce interconnect resistance:
- a. Routing in upper (thicker) metals
 - b. Routing in lower layers
 - c. Increasing the drive strength
 - d. None of the above
64. Having a trace wider than the minimum width_____.
- a. Reduces interconnect resistance without causing a significant increase in the parasitic capacitance
 - b. Increases interconnect resistance without causing a significant increase in the parasitic capacitance
 - c. Reduces interconnect resistance with increase in the parasitic capacitance
 - d. Increases interconnect resistance with decrease in the parasitic capacitance
65. Net capacitive load is _____.
- a. Sum of pin capacitance loads of every fan-out of the net
 - b. Average of pin capacitance loads of every fan-out of the net
 - c. Square of sum of pin capacitance loads of every fan-out of the net
 - d. None of the above

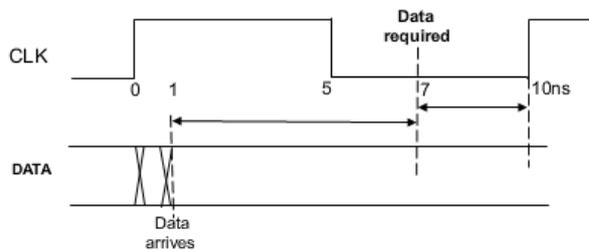
66. Elmore delays are applicable for RC trees, which:
- Have a single input node
 - Does not have any resistive loops
 - All capacitances are between a node and a ground
 - All of the above

67. For the following figure, what is the Elmore delay equation:



- $\sum_{i=1, N} C_i (\sum_{j=1, i} R_j)$
- $\sum_{i=1, N} C_i (\sum_{j=1, i} R_{j+1})$
- $\sum_{i=1, N} C_i (\sum_{j=1, i} R_j - 1)$
- $\sum_{i=1, N} C_i (\sum_{j=1, i} R_j / 1)$

68. Calculate the Slack for the following figure, if T_{setup} of capture flop = 3ns:



- 6 ns
- 7 ns
- 8 ns
- 9 ns

69. For each setup relationship, what type of hold checks will be performed by PrimeTime?

- a. The data launched by the setup launch edge must not be captured by the previous capture edge
 - b. The data launched by the next launch edge must not be captured by the setup capture edge
 - c. Both a and b
 - d. None of the above
70. State whether the following statement is either True or False. Virtual clock exists but isn't associated with any pin or port. It is used as a reference in STA analysis to specify input and output delays relative to a clock.
- a. True
 - b. False
71. If a path exists between two multiplexed logic blocks that are never selected at the same time, then that path is considered as _____.
- a. Critical Path
 - b. False Path
 - c. Multi-Cycle Path
 - d. None of the above
72. Select the correct statement with respect to the false path:
- a. Path between flip-flops belonging to two clock domains that are asynchronous with respect to each other
 - b. Path between flip-flops belonging to same clock domain that are asynchronous with respect to each other
 - c. Path between flip-flops belonging to two clock domains that are synchronous with respect to each other
 - d. Path between flip-flops belonging to same clock domain that are asynchronous with respect to each other
73. State whether the following statement is either True or False. In operating conditions, Value related to the scaling of device parameters resulting from variations in the fabrication process represent process derating factors.
- a. True
 - b. False
74. State whether the following statement is either True or False. A process number less than the nominal value usually results in smaller delays.
- a. True
 - b. False
75. In operating conditions, Interconnect model type defines:
- a. RC tree topology that EDA tool uses to estimate net capacitance and resistance during pre-layout analysis
 - b. Interconnect delays

- c. Cell delays
- d. None of the above

76. In On-Chip variation (OCV) Mode, for Setup check, EDA tool uses _____delays for the launch clock path and data path, _____ delays for capture clock path.

- a. Maximum, Minimum
- b. Minimum, Maximum
- c. Maximum, Maximum
- d. Minimum, Minimum

77. In On-Chip variation (OCV) Mode, for Hold Check, EDA tool uses _____delays for the launch clock path & data path, _____ delays for capture clock path

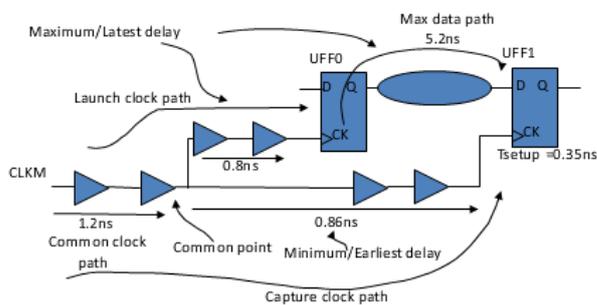
- a. Maximum, Minimum
- b. Maximum, Maximum
- c. Minimum, Minimum
- d. Minimum, Maximum

78. Apart from the variations in the process parameters, different portions of the design may also see different power supply voltage and temperature. These differences can arise due to:

- i) IR drop variation
- ii) Voltage threshold variation of PMOS or NMOS device
- iii) Channel length variation
- iv) Interconnect metal etch or thickness variations

- a. i) and ii)
- b. i) and iii)
- c. iii) and iv)
- d. All of the above

79. For the figure shown below, calculate the minimum clock period:



- a. 5.49ns
- b. 5.48ns

- c. 5.47ns
- d. 5.46ns

80. Clock re-convergence pessimism is an accuracy limitation that occurs when:
- a. Two different clock paths partially share a common physical path segment and the shared segment is assumed to have a minimum delay for one path and maximum delay for other path
 - b. Two different clock paths partially share a different physical path segment and each segment is assumed to have a minimum delay for one path and maximum delay for other path
 - c. None of the above
 - d. Both a and b
81. State whether the following statement is either True or False. There is a timing path between d and clk in D flip flop.
- a. True
 - b. False
82. State whether the following statement is either True or False. There is a timing path between d and clk in D latch.
- a. True
 - b. False
83. State whether the following statement is either True or False. Static timing analysis performs functionality check.
- a. True
 - b. False
84. Parasitic interconnect corners are governed by the variations in:
- a. Metal width
 - b. Metal etch
 - c. Both a and b
 - d. None of the above
85. What are the reasons for noise playing an important role in deep sub-micron technologies?
- a. Increasing number of metal layers and high routing density
 - b. Lower supply voltage and vertically dominant metal aspect ratio
 - c. Both a and b
 - d. None of the above
86. What are the effects as the result of cross talk?
- a. Noise effect on a static signal which will change the expected logical value
 - b. Cross talk delay
 - c. Both a and b

- d. None of the above
87. State whether the following statement is either True or False. A steady signal net can have a glitch due to charged transferred by the switching aggressors through the coupling capacitances.
- a. True
 - b. False
88. If coupling capacitance is high, magnitude of the glitch will be:
- a. Smaller
 - b. Larger
 - c. No Change
 - d. Cannot be determined
89. State whether the following statement is either True or False. In general, faster slew is due to higher output drive strength for the cell driving the aggressor net.
- a. True
 - b. False
90. The magnitude of the glitch caused is depended upon:
- a. Slew of the aggressor net
 - b. Victim net grounded capacitance
 - c. Victim net driving strength
 - d. All of the above
91. Overshoot glitch occurs when:
- a. A rising aggressor couples to a victim net which is steady high
 - b. A falling aggressor couples to a victim net which is steady low
 - c. A rising aggressor couples to a victim net which is steady low
 - d. None of the above
92. Which check is used for glitch magnitude and refers to DC noise limits on the input of a cell while ensuring proper logic functionality:
- a. DC noise margin
 - b. AC noise margin
 - c. Both a and b
 - d. None of the above
93. Consider a victim net V coupled to aggressor nets A1, A2, A3 and A4. During STA, is it possible that A1, A2 and A4 contribute to rising and overshoot glitches, whereas only A2 and A3 contribute to undershoot and falling glitches:
- a. Yes, it is possible
 - b. No, it is not possible
94. State whether the following statement is either True or False. The charge required for the coupling capacitance is larger when the coupled net and victim net are switching in the opposite directions.

- a. True
- b. False

95. The basic STA analysis is conservative in the sense that:

- a. It will overestimate the delay of long paths in the circuit and underestimate the delay of short paths and will not suffer from hold time violations
- b. It will underestimate the delay of long paths in the circuit and overestimate the delay of short paths and will not suffer from hold time violations
- c. It will overestimate the delay of long paths in the circuit and underestimate the delay of short paths and will not suffer from setup time violations
- d. It will underestimate the delay of long paths in the circuit and overestimate the delay of short paths and will not suffer from setup time violations

96. Formal verification involves:

- a. Logic equivalence checking
- b. Ignores timing information
- c. Both a and b
- d. None of the above

97. Select the correct order for Equivalence Checking:

- i) Match
 - ii) Read
 - iii) Debug
 - iv) Verification
- a.i), ii), iii) and iv)
b.ii), i), iv) and iii)
c.ii), iv), iii) and i)
d.i), iii), ii) and iv)

98. What are the different Formal Verification Components:

- a. Net driven by Multiple Drivers
- b. Inputs of a Black Box
- c. Logic Cone
- d. All of the above

99. During the read process in Equivalence Checking:

- a. Reference and Implementation designs are automatically segmented into manageable sections called "Logic Cones"
- b. Reference and Implementation designs are automatically segmented into manageable sections called "Compare Points"
- c. Both a and b
- d. None of the above

100. The output border of a logic cone is referred as:
- a. Black Box
 - b. Compare Point**
 - c. Verification Point
 - d. Debug Point