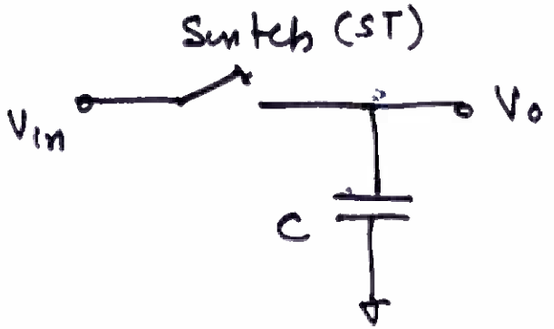
Sample and Hold Circuit



Initial condn: $V_o = 0$ and ST = 0 (open)

V_{in} is impressed and ST closes.

Capacitor charges towards $V_{in}(t)$ value at $t=t_1$. Now ST opens.

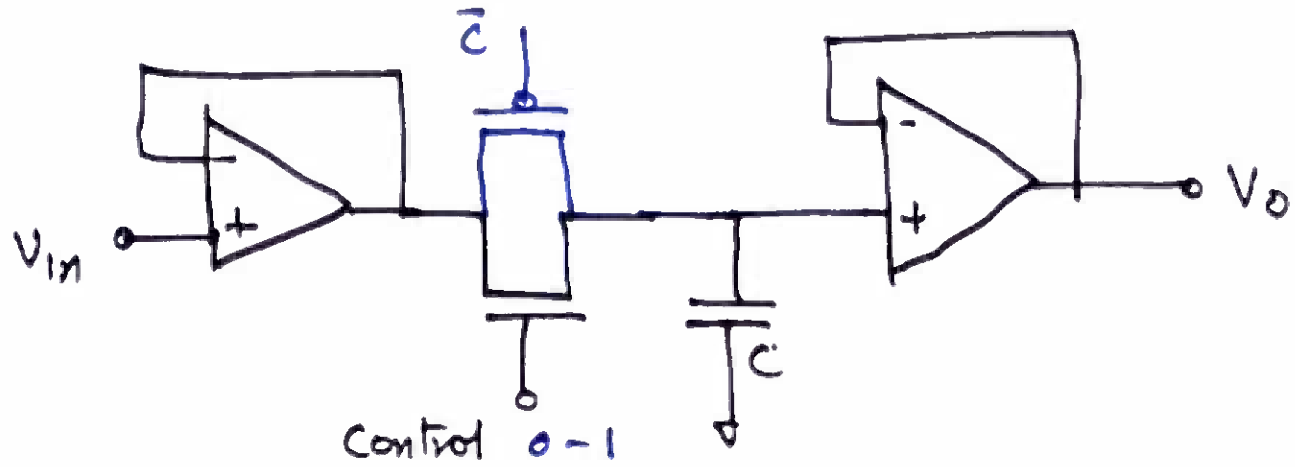
Then $V_{o1} = V_c(t) = V_c(t_1) = V_{in}(t_1)$

Till 'ST' closes output is 'Held' to V_{o1}.

When 'ST' closes, V_o tries to follow V_{in} (with last initial condn.)

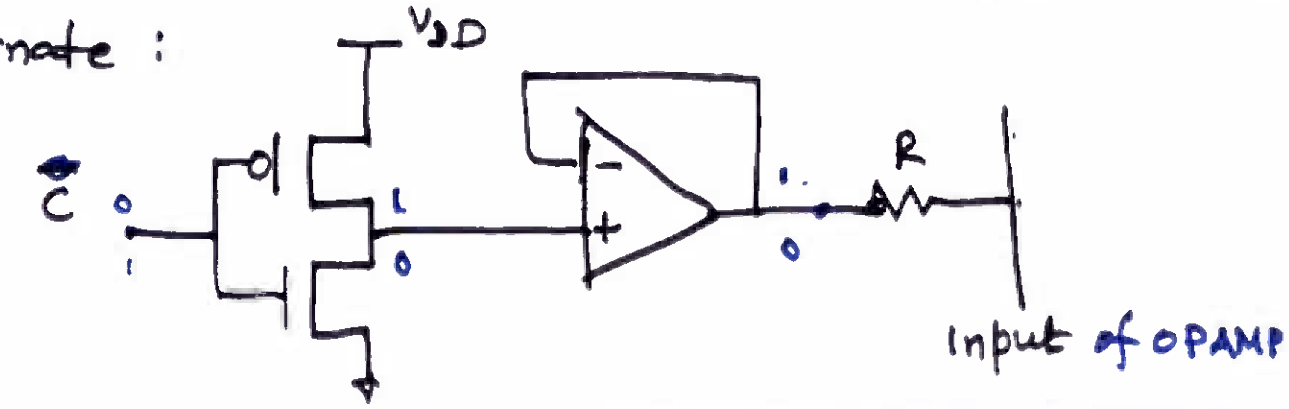
This we say 'Sampling'

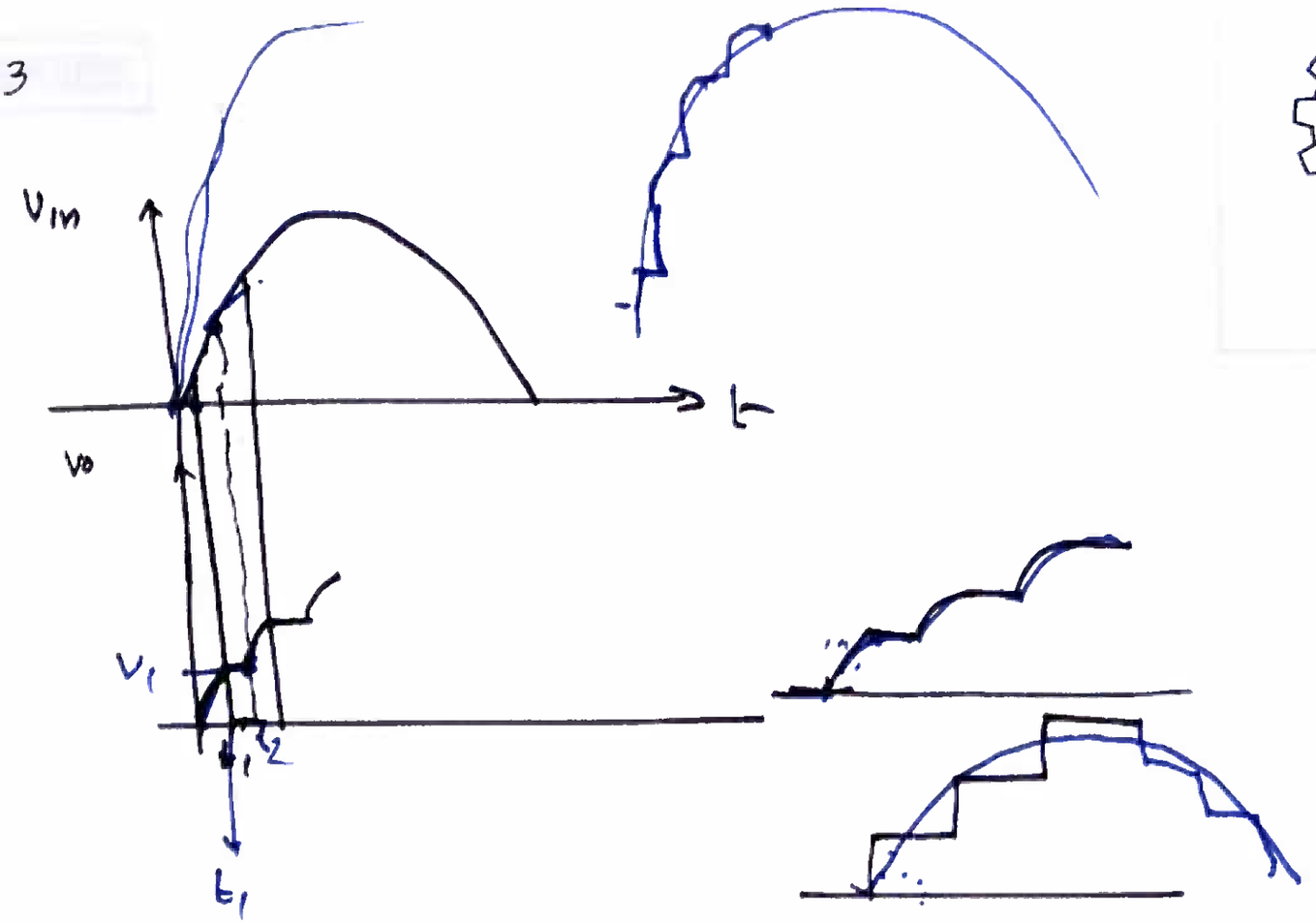
A simple S-H Circuit is



MOS Transistor in common Gate mode acts like a Switch.

Alternate :





Digital to Analog Converter
(D/A Converter or DAC)

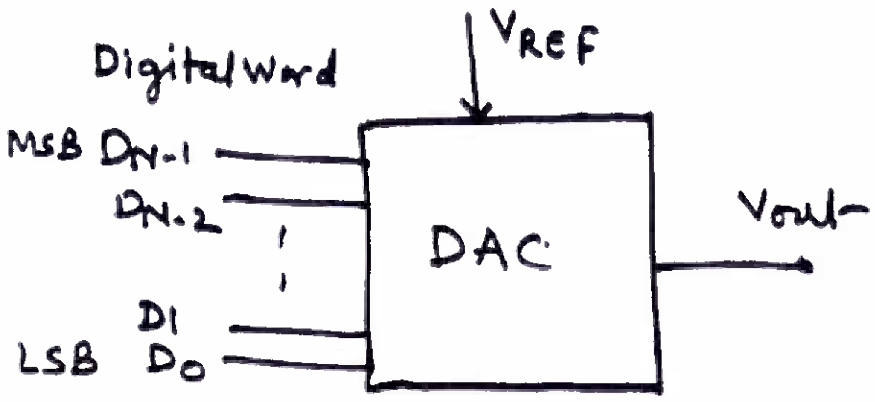
Lets assume Digital word is in Binary Code Corresponding to a N-bit binary code, we have Analog Voltage as V_0

$$V_0 = \left(2^{N-1} a_{N-1} + 2^{N-2} a_{N-2} \cdots 2^2 a_2 + 2^1 a_1 + 2^0 a_0 \right) V$$

(V: Const.)

$$= \left(a_{N-1} + \frac{1}{2} a_{N-2} + \cdots \frac{1}{2^{N-2}} a_1 + \frac{1}{2^{N-1}} a_0 \right) 2^{N-1} V$$

DAC specifications



Typically, the output of DAC is a fraction F of V_{REF}.

i.e. $V_{out} = F V_{REF}$

Word D is N-bit wide, then

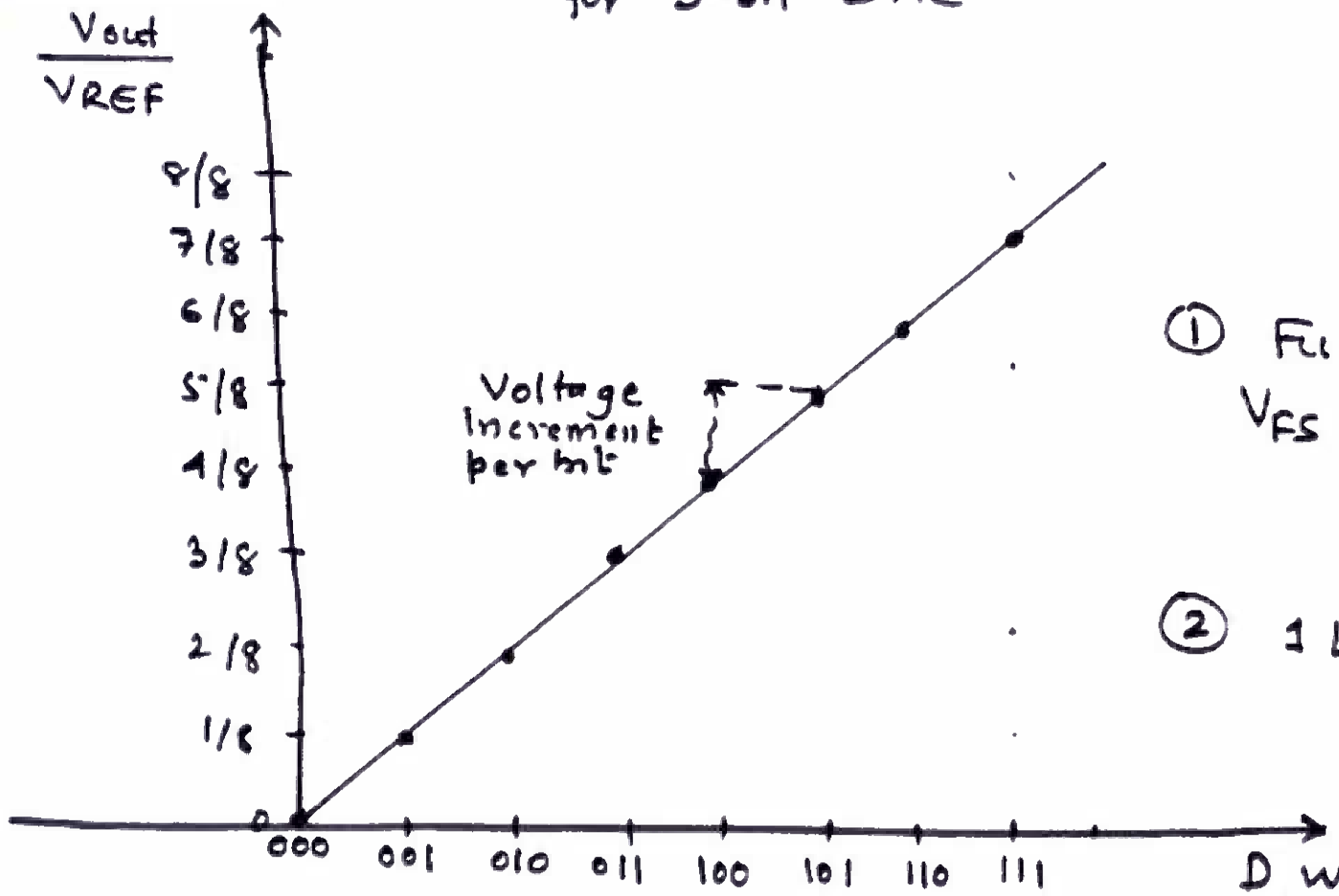
No. of Input Combinations $= 2^N$

A 4bit DAC has $2^4 = 16$ Input Combinations

Clearly a 4-bit DAC has 4bit Resolution, which means each input (16) should have distinct Analog output

Slide No: 6

Ideal Transfer Characteristics for 3-bit DAC



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① Full Scale Voltage

$$V_{FS} = \frac{2^N - 1}{2^N} V_{REF}$$

$$= \frac{7}{8} V_{REF} \quad \text{3 bit case}$$

② $1\ LSB = \frac{V_{REF}}{2^N} \left(= \frac{5}{8} V\right)$

Then $F = \frac{D}{2^N}$

If D is 4 bit wide $f = \frac{8}{2^4} = \frac{8}{16} = \frac{1}{2}$

1000

8

Similarly 3 bit DAC, $F = \frac{4}{2^3} = \frac{4}{8} = 1/2$

(100)

4

If $V_{REF} = 5V$ then $V_o = \frac{1}{2} \times 5V = 2.5V$

$\therefore$ Resolution = 2.5 V

i.e. each bit of 3bit DAC (000, 001 - - 111) is separated by 2.5V (for $V_{REF} = 5V$)

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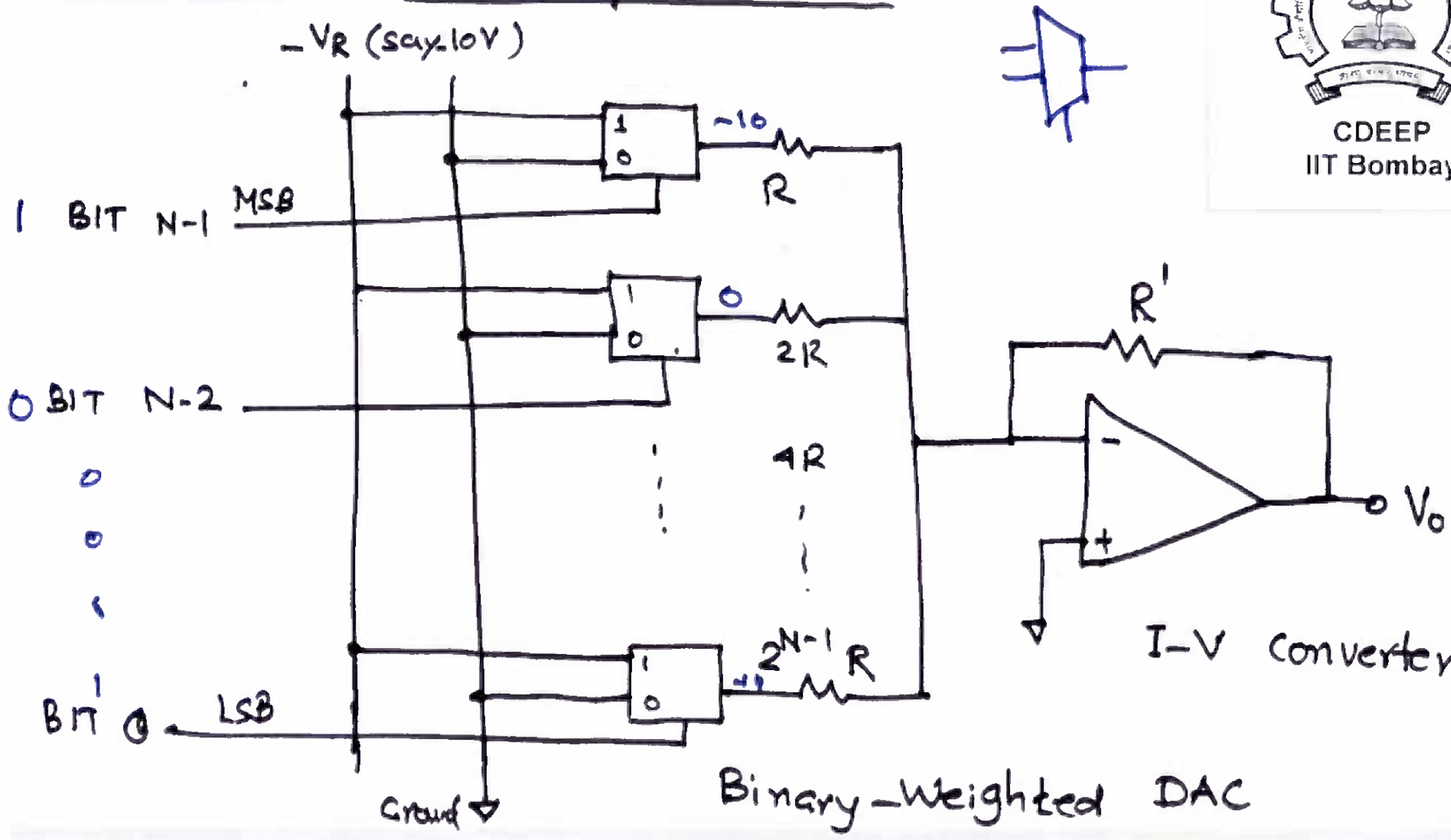
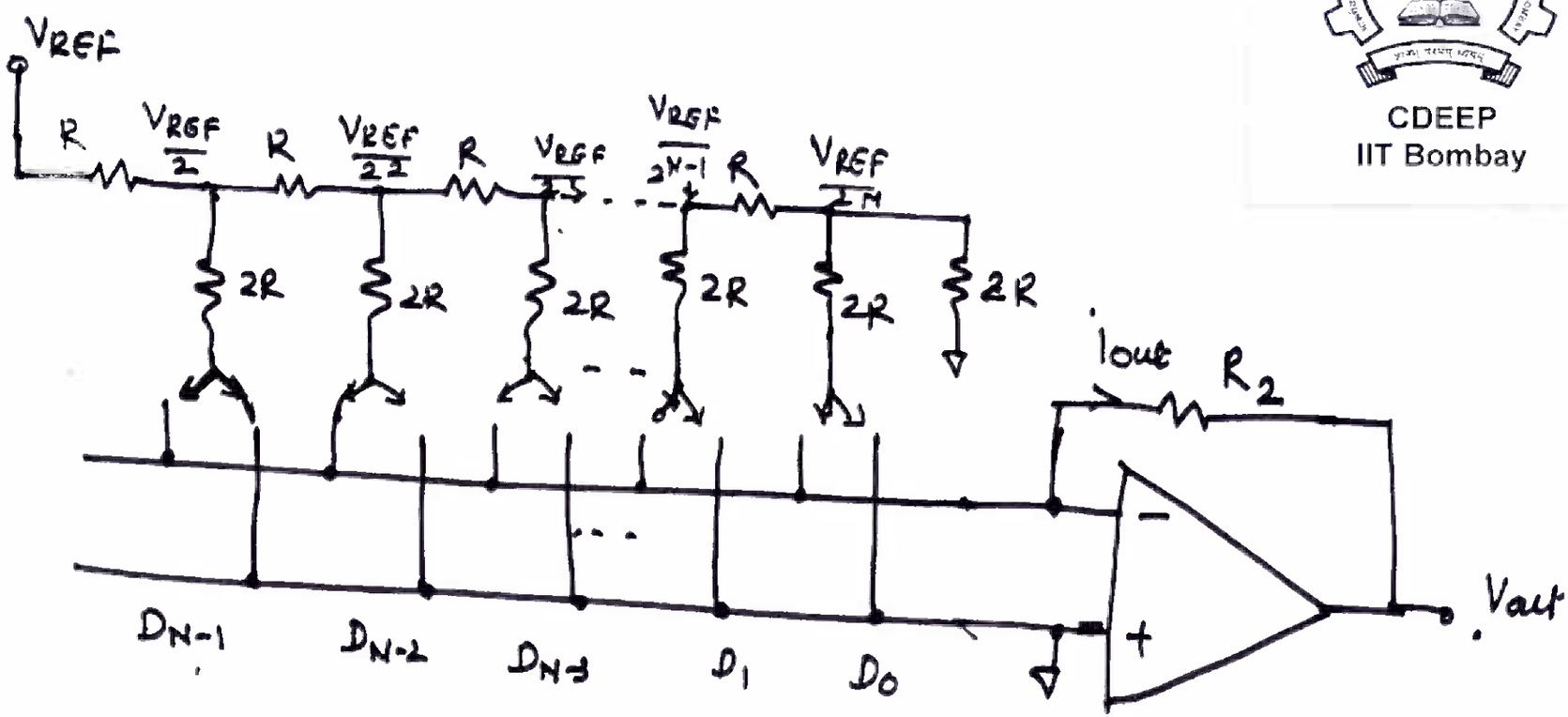
DAC implementation



Binary-Weighted DAC

R-2R DAC

SPDT



$$V_o = -I_{out} R_2 \quad , \quad I_{out} = \sum_{k=0}^{N-1} D_k \frac{V_{REF}}{2^{N-k}} \cdot \frac{1}{2R}$$

A to D converters (ADCs)

(i) Counting ADC

(ii) Successive Approximation ADC

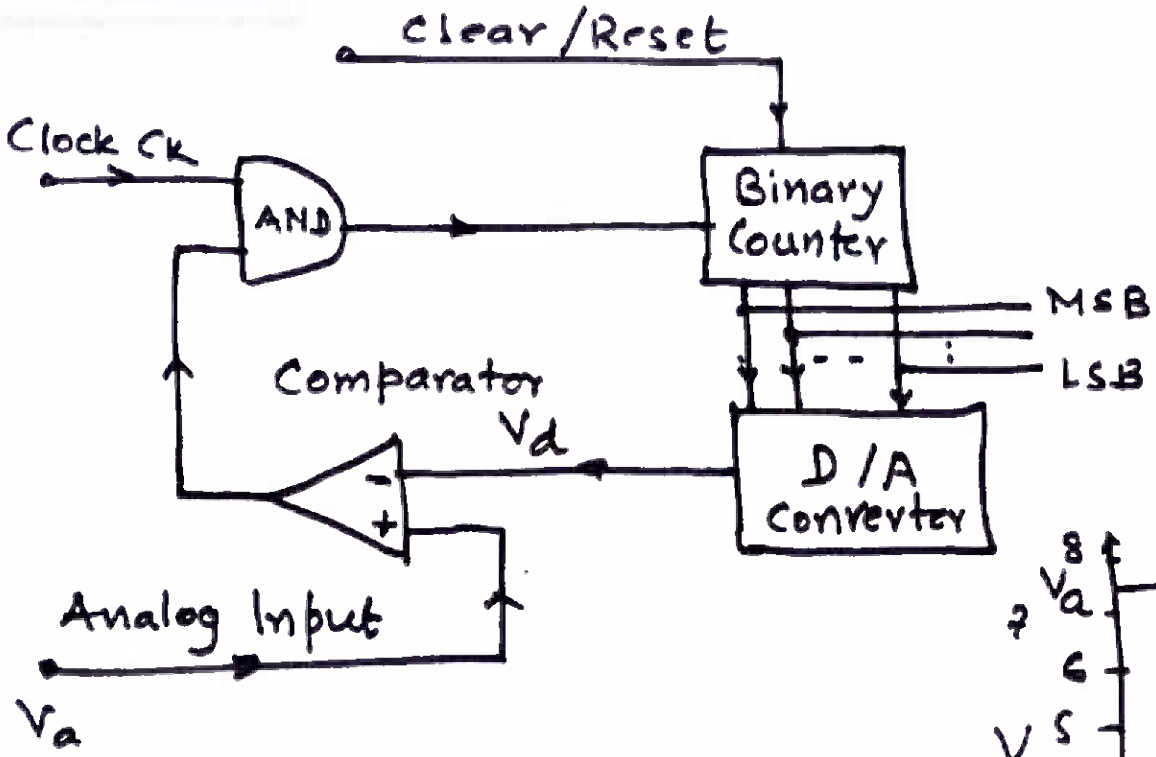
(iii) Flash ADC

(iv) Dual-Slope ADC. / Single Slope

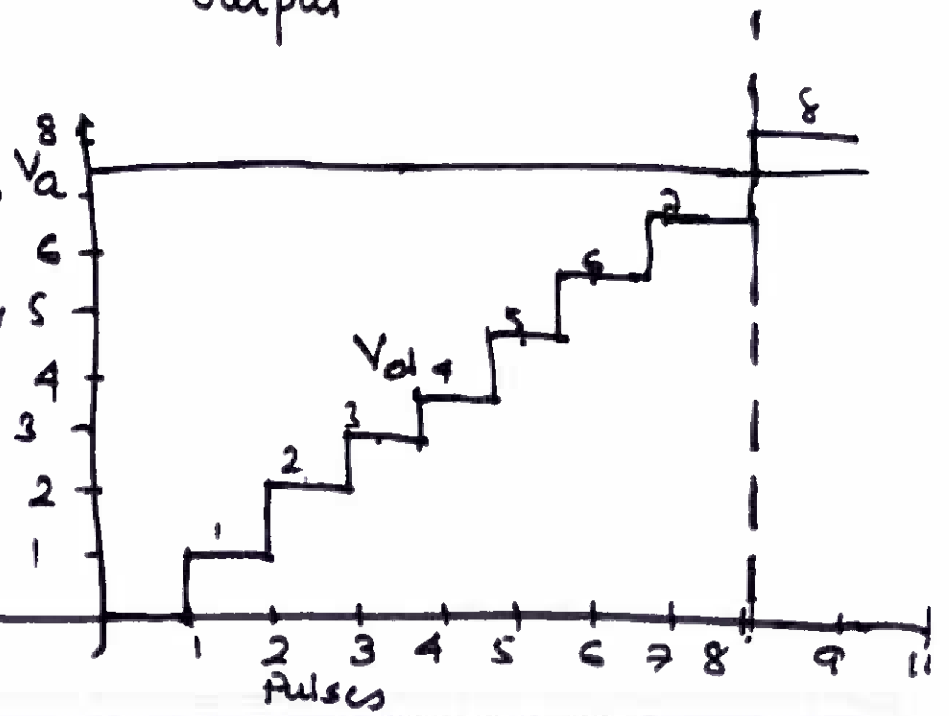
(v) Multi-step

(vi) Pipelined

Counting ADC



Digital output



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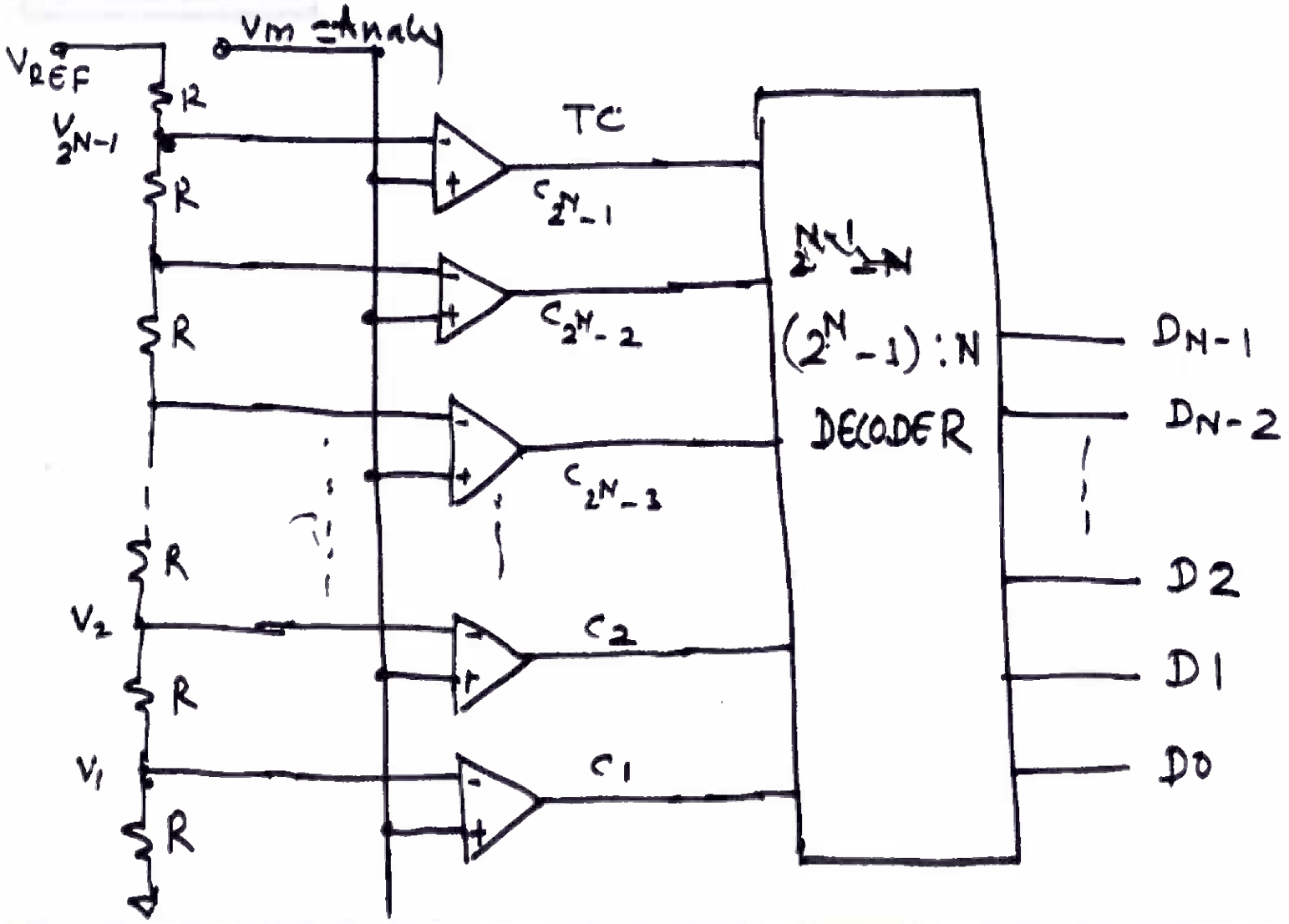
Flash ADC



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For 3bit Flash ADC

Each Tap has voltage $= \frac{R}{8R} V_{REF} = \frac{1}{8} V_{REF}$

For $V_{REF} = 5V$, Each Tap has voltage $= \frac{5}{8} = 0.625V$

$\therefore V_1 = 0.625V$, $V_2 = 1.25V$, $\therefore V_7 = \frac{7}{8} \times 5 = 4.375V$

Let us say $V_{in} = 3V$

Then C_{2^N-1} — C_1 $= 0001111 \Rightarrow \underset{\text{coded to Binary}}{100} \rightarrow 4$

	Binary	TC
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0111