Sample and Hold Circuit

Switch \( ST \)

Vin \( \rightarrow \) V0

C

Initial condn: \( V_0 = 0 \)
and \( ST = 0 \) (open)

Vin is impressed and \( ST \) closes.

Capacitor charges towards \( Vin(t) \) value at \( t = t_1 \). Now \( ST \) opens.

Then \( V_{01} = V_c(t_1) = V_c(t_1) = V_m(t_1) \)

Till \( ST \) closes output is 'Held' to \( V_{01} \).

When \( ST \) closes, \( V_0 \) tries to follow \( Vin \) (with last initial condn.)

This we say 'Sampling'.
A simple S-H Circuit is

MOS Transistor in common gate mode acts like a Switch.

Alternate:

Input of OPAMP
Digital to Analog Converter
(D/A Converter or DAC)

Let's assume Digital word is in Binary Code corresponding to a N-bit binary code, we have Analog Voltage as $V_0$

$$V_0 = (2^{N-1}a_{N-1} + 2^{N-2}a_{N-2} + \cdots + 2a_2 + \frac{1}{2}a_1 + \frac{1}{2^{N-1}}a_0) V$$

$$= (a_{N-1} + \frac{1}{2}a_{N-2} + \cdots + \frac{1}{2^{N-2}}a_1 + \frac{1}{2^{N-1}}a_0) 2^{N-1} V$$

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DAC specifications

Typically, the output of DAC is a fraction \( F \) of \( V_{REF} \).

\[ \text{Vout} = F \cdot V_{REF} \]

Word \( D \) is \( N \)-bit wide, then

No. of Input Combinations = \( 2^N \)

A 4-bit DAC has \( 2^4 = 16 \) Input Combinations

Clearly a 4-bit DAC has 4-bit Resolution, which means each input should have distinct Analog Output.
Ideal Transfer Characteristics for 3-bit DAC

1. Full Scale Voltage
   \[ V_{FS} = \frac{2^N - 1}{2^N} V_{REF} \]
   \[ = \frac{7}{8} V_{REF} \]

2. 1 LSB
   \[ 1 \text{ LSB} = \frac{V_{REF}}{2^N} \]
   \[ = \frac{5}{8} \] 3-bit range

D word width 3-bit wide
Then \( F = \frac{D}{2^N} \)

If \( D \) is a bit wide, \( F = \frac{8}{2^4} = \frac{8}{16} = \frac{1}{2} \)

1000
\[
\downarrow \\
8
\]

Similarly 3-bit DAC, \( F = \frac{4}{2^3} = \frac{4}{8} = \frac{1}{2} \)

1

\[
\downarrow \\
(100)
\]

If \( V_{REF} = 5V \) then \( V_0 = \frac{1}{2} \times 5V = 2.5V \)

\[
\text{Resolution} = 2.5V
\]

\( i.e. \) each bit of 8-bit DAC (000, 001, ..., 111) is separated by 2.5V (for \( V_{REF} = 5V \))
DAC implementation

1 BIT N-1

0 BIT N-2

0 BIT 0

MSB

LSB

-VR (say 10V)

\[ R \]

\[ 2R \]

\[ 4R \]

\[ 2^{N-1} R \]

I-V converter

Binary-Weighted DAC

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R-2R DAC

\[ V_0 = - \frac{Q_{out}}{R_2}, \quad I_{out} = \sum_{k=0}^{N-1} D_k \cdot \frac{V_{REF}}{2^{N-k-1}} \cdot \frac{1}{2R} \]
A to D Converters (ADCs)

(i) Counting ADC

(ii) Successive Approximation ADC

(iii) Flash ADC

(iv) Dual-Slope ADC / Single Slope

(v) Multi-step

(vi) Pipelined
Counting ADC

Clear/Reset

Clock CK

AND

Comparator

Vd

Binary Counter

Digital output

MSB

LSB

D/A converter

Analog Input

Va

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Flash ADC

\[ V_{REF} \]

\[ V_{2^{N-1}} \]

\[ V_R \]

\[ V_2 \]

\[ V_1 \]

\[ T_{C} \]

\[ 2^{N-1} \]

\[ 2^{N-2} \]

\[ 2^{N-1} \]

\[ 2 \]

\[ 1 \]

\[ D_{N-1} \]

\[ D_{N-2} \]

\[ D_2 \]

\[ D_1 \]

\[ D_0 \]

Digital output
For 3-bit Flash ADC

Each Tap has voltage \( V_{\text{ref}} = \frac{R}{8R} V_{\text{REF}} = \frac{1}{8} V_{\text{REF}} \)

For \( V_{\text{REF}} = 5 \text{V} \), Each Tap has voltage \( \frac{5}{8} = 0.625 \text{V} \)

\( v_1 = 0.625 \text{V}, \quad v_2 = 1.25 \text{V}, \quad v_7 = \frac{7 \times 5}{8} = 4.375 \text{V} \)

Let us say \( V_{\text{IN}} = 3 \text{V} \)

Then \( \begin{array}{c}
  \text{Binary} \\
  0 \\
  1 \\
  2 \\
  3
\end{array} \begin{array}{c}
  \text{TC} \\
  0000 \\
  0001 \\
  0010 \\
  0011
\end{array} \)

\( \Rightarrow \begin{array}{c}
  \text{Encoded to Binary} \\
  100
\end{array} \)