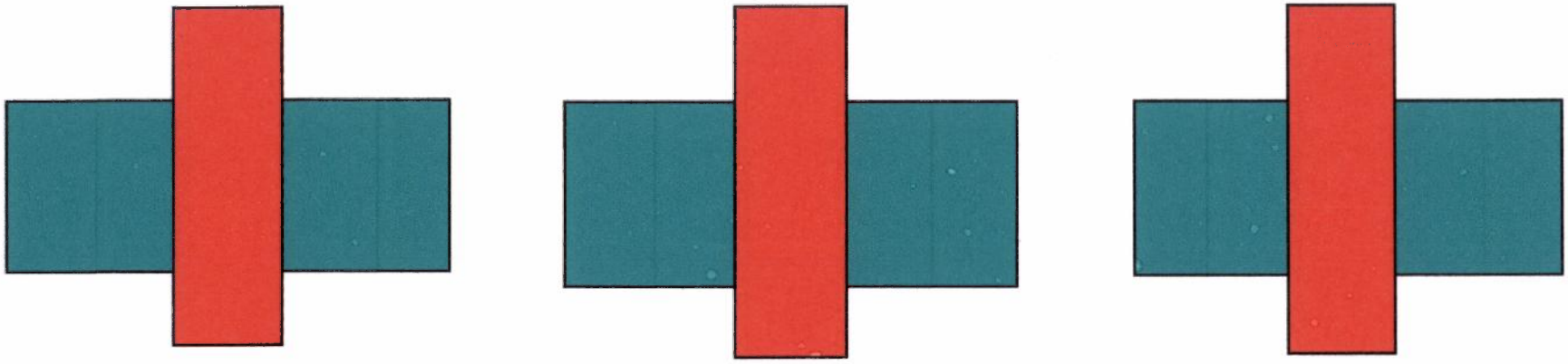
Transistor mismatch in deep sub-micron technology

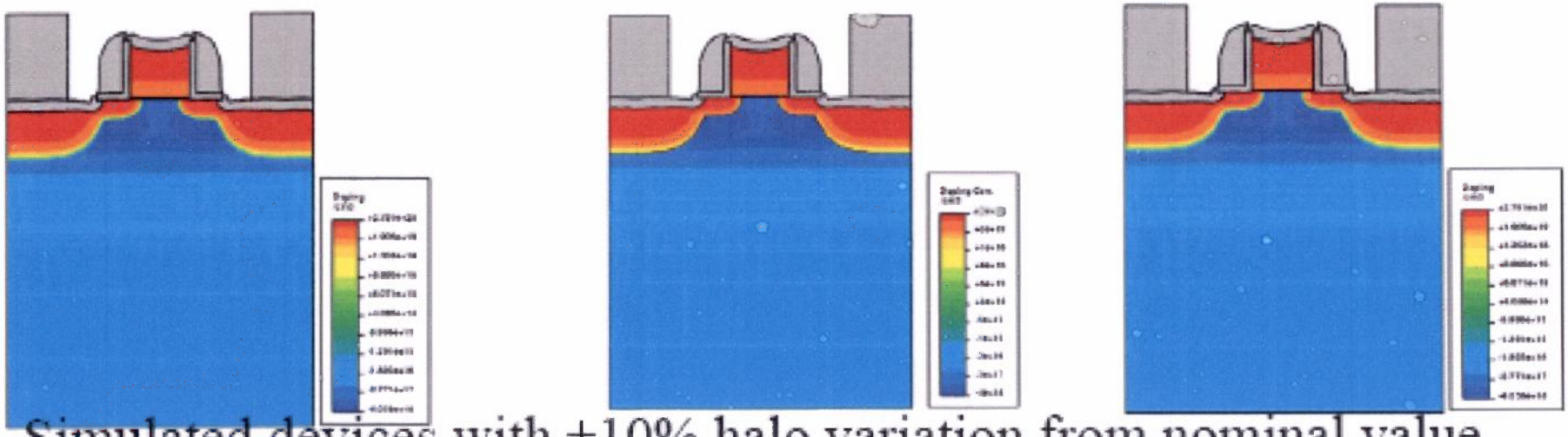
- Factors causing transistor mismatch
- Modeling the transistor mismatch
- Controlling mismatch effect at process/device level
- Impact of transistor mismatch in sense-amplifier design
- Controlling mismatch effect at circuit level

Transistor Mismatch Effects

3 identical transistors in a chip at the circuit design phase



The structure of 3 transistors after the completion of IC processing



Simulated devices with ±10% halo variation from nominal value

Factors Causing Mismatch

1.*Intrinsic type*

- Discrete dopant effect
- Interface state density fluctuations

2.*Extrinsic type due to random variation in:*

- Gate length and width
- Oxide thickness
- Implant dose
- Implant energy
- Anneal temperature
- Gate & S/D overlap
- Spacer thickness

Device parameters affected by process parameters

- I_{off}, the leakage current
- I_{on}, the saturation current
- V_t, the threshold voltage
- S, the Sub threshold slope
- g_m, the Tranconductance.
- Various R s, C s and parasitics