LEAKAGE CURRENT
CONTROL
BY
CIRCUIT TECHNIQUES
DVTS

Dynamic Voltage & Threshold Scaling

DVTS is improved version of DVS as it can be achieved at most technology nodes (scaling)
DVS

We have a Single Loop here.

$V_{dd}$ IS ADJUSTED FOR SPEED PERFORMANCE

VOLTAGE - FREQUENCY RELATION STORED IN LOOK-UP Table

"MOST COMMONLY USED TECHNIQUE"
(b) DVC gets this information and which then allows $V_{dd}$ to regulate. Condition that this meets critically path delay

(c) Delay is fed back to DFC. Two loops achieve stable values for $V_{dd}$ and $f$
Two closed-loops in DVFS

1. Dynamic Voltage Control → DVC

2. Dynamic Frequency Control → DFC

Steps in Control:

a. DFC monitors chip activity

⇒ decides frequency to work at
'Dynamic Voltage and Frequency Scaling'

**DVFS**

We have \( P_{\text{dynamic}} \propto V_{\text{DD}}^2 \propto f \)

Reducing \( V_{\text{DD}} \) => \( P_{\text{dynamic}} \) REDUCES

\( \Rightarrow \) REDUCES \( P_{\text{LEAKAGE}} \)

AS \( V_{\text{DD}} \downarrow \) reduces \( V_{\text{TH}} \) through Change in DIBL
ADAPTIVE BIASING
VARIABLE VTH CMOS

\[ \text{(VTCMOS)} \]

[A] ACTIVE MODE $\rightarrow$ BACK-BIAS
TRANSISTORS HAVE LOW VTH.

[B] 'OFF STAND-BY' $\rightarrow$ BACK-BIAS
SET TO HIGH
REVERSE BIAS
TRANSISTORS ARE NOW HAVING HIGHER VTH $\Rightarrow$ LOWER LEAKAGE
IN 'OFF' MODE SL = 1

MP AND MN ARE OFF WITH LOWER LEAKAGE WITH ADDITIONAL SERIES HIGH $V_{TH}$ TRANSISTORS

DISADVANTAGES

1. LARGE AREA

2. SLOWER PERFORMANCE
MULTI THRESHOLD-VOLTAGE CMOS (MTCMOS)

AT $SL = 0$ (Active Mode)
- $MP$ - ON
- $MN$ - ON

SLEEP TRANSISTORS ARE LARGE SIZE
HIGH $V_{TH}$ ONES

"We create $V_{DDV}$ & $V_{SSV}$"
MULTIPLE BODY BIAS

Substrate Bias Changes \( V_{th} \)

\[
V_{th}(V_{SB}) = V_{TO} + \gamma \left[ (V_{SB} + 2\phi_F)^{\frac{1}{2}} - (2\phi_F)^{\frac{1}{2}} \right]
\]

\( \gamma = \frac{[2K_S\varepsilon_0qN_B]^{\frac{1}{2}}}{\frac{C_{ox}}{C_{ox}}} \) = Body Bias Coeff.

Applying Appropriate Body Bias to Various Transistors, Multiple \( V_{th} \) Transistors are Created.
2(b) GATE-OXIDE CHANGE LEADS TO
CHANGE IN $C_{ox}$.

$V_{th} \propto t_{ox}$

ASSIGN LOWER $V_{th}$ TO
TRANSISTORS IN CRITICAL PATH
OTHER TRANSISTORS HAVE
HIGHER $V_{th}$ LEADING TO LOWER
SUB-THRESHOLD CURRENTS.
2. MULTIPLE \( V_{TH} \) TECHNIQUE

(a) CHANNEL DOING VARIATES FOR DIFFERENT \( V_{TH} \) TRANSISTORS

\[
V_{TH} = \phi_{MS} \pm 2\phi_F - \frac{Q_{ox}}{C_{ox}} - \frac{Q_B}{C_{ox}}
\]

\( \phi_{MS} = \text{METAL-SEMICONDUCTOR WORK FUNCTION DIFFERENCE} \)

\( \phi_F = \frac{kT}{e} \ln \frac{N_B}{N_i} \), \( N_B \) - SUBSTRATE DOPING
$Q_{ox}$ is fixed positive charge density

$C_{ox} = \frac{E_{ox}}{t_{ox}}$, \( t_{ox} \) - Oxide Thickness
\( E_{ox} \) - Oxide Permittivity

$Q_B = \pm q N_B X_{DMAX}$, \( X_{DMAX} \) - Depletion Width

$V_{TH} \propto \sqrt{N_B}$

$X_{DM} = \sqrt{\frac{2 k_\Phi E_0}{e N_B}}$
(iii) \( V_{DS_2} = V_D - V_{S_2} = V_D - V_M \)

Since \( V_M \) is positive, \( V_{DS_2} \) is smaller. Hence \( V_{TH_2} \) increases due to lowered DIBL value.

In all three cases one observes reduction in sub-threshold current \( \Rightarrow \) reduced leakage power.
(i) \[ V_{GS_2} = V_{G2} - V_{S2} = V_{G2} - V_M \]
\[ = 0 - V_M = -V_M \]

Subthreshold current of M2 reduces

Hence NET LEAKAGE CURRENT REDUCES

(ii) \[ V_{BS_2} = V_{B2} - V_{S2} = -V_M \]

Extra Reverse Back-Bias Enhances \( V_{TH} \) of M2. THIS LEADS TO REDUCED LEAKAGE CURRENT
LEAKAGE CONTROL

1. Stack Effect:
   ⇒ SELF REVERSE BIAS

2-INPUT NAND → AS EXAMPLE

   WHEN A = B = 0
   M2 & M1 → OFF
   M3 & M4 → ON

LEAKAGE CURRENT Flows
FROM VDD to VSS
Due to stacking of NMOS transistors M1 & M2, we observe that at node M between M1 & M2, has voltage +V_m, due to flow of leakage current. Positive V_m has THREE Effects leading to lowering of leakage current.
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   K. Yeo & K. Roy

3. Digital IC - Design Perspective
   J.M. Rabaey, A. Chandrakasan
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4. CMOS VLSI -
   Eshraghian & Waste