Continuing..

**PRINTED WIRING BOARD TECHNOLOGIES**
Key advantages

- **Photovia**: Lowest cost due to parallel processing
- **CO₂ laser**: Fastest drill rate, any dielectric can be drilled, to open copper on the copper plane—need to switch to chemical or YAG
- ***YAG laser**: Copper can be drilled, smallest holes possible, any dielectric can be drilled
- **Plasma**: Very cost-effective parallel process, high yield, environmentally clean, almost any dielectric material can be processed

Yttrium aluminium garnet (YAG), $Y_3Al_2(AlO_4)_3$

Nd:YAG (neodymium-doped yttrium aluminium garnet); Nd:$Y_3Al_5O_{12}$

*Fig. source: Garnet encyclopedia: www.absoluteastronomy.com*
IBM’s Surface Laminar Circuit

• Surface Laminar Circuit™: “An Organic Packaging Solution”

• SLC structure has two major parts
  ✓ FR 4 substrate and
  ✓ SLC layer built up (SBU technology)

• It is a methodology to have a PCB as a MCM-L and use existing PCB technologies
Outline

• Use of photo-polymer to build additional layers of dielectric on a normal PWB core
• Photo-imaging creates blind and buried vias
• Eliminates mechanical NC drilling
• Build up on both sides
• No glass fabric in the polymer; hence light and thin board
• 2-4 additional layers can be built
• Now referred to as SBU technology
  – Sequential Build-Up Technology
Features

- High density
  - 1mil via
  - 1mil line and space
- SMT pads on blind photo via
- More design freedom, routing capability
- Ability to accommodate flip chip and bare die; hence classifies under MCM-L
- Used currently in video camcorders and telecommunication products
• PCMCIA Card
  - 0.7mm thick with 6 layers
  - 2 build up layers one side of a 4 layer FR4
  - FCA Chip 1:
    • 7.5mm square
  - FCA Chip 2
    • 4.0 x 10.8 mm square

• Single chip BGA
  - 25mm square
  - 0.8mm thick with 6 layers
  - 1 build up layer on both sides of 4 layer FR4
  - FCA Chip:
    • 8.05 x 8.1 mm
    • smallest via ~90um

Source: Dr. Tsukada, IBM Yasu, Japan
Sequential Build Up Process Flow

1. CHOOSE SUBSTRATE; SURFACE PREPARATION
2. COAT PHOTORESIST AND PRE-BAKE
3. PHOTO-EXPOSE, DEVELOP, CURE USING MASK
4. SUB-ETCH COPPER LAYER (LAYER 1)
5. STRIP PHOTORESIST
6. APPLY PHOTO-POLYMER DIELECTRIC
7. PHOTO-EXPOSE, DEVELOP, FINAL CURE
8. METALLIZATION PROCESS
   - ELECTROLESS PLATING, ELECTROPLATING (LAYER 2)
8 Layer -1+[3+3]+1

Build-up Layer
Core Material Layers
Build-up Layer
Signal

12 Layer - 2+8+2

Build-up Layers
Core Material Layers
Build-up Layers
<table>
<thead>
<tr>
<th>characteristic</th>
<th>photo-liquid</th>
<th>photo-film</th>
<th>laser-RCC</th>
<th>Laser-MP</th>
<th>plasma</th>
</tr>
</thead>
<tbody>
<tr>
<td>dielectric cost</td>
<td>medium/high</td>
<td>high</td>
<td>high</td>
<td>medium/high</td>
<td>high</td>
</tr>
<tr>
<td>via size (lab)</td>
<td>50μm</td>
<td>100μm</td>
<td>75μm</td>
<td>100μm</td>
<td>100μm</td>
</tr>
<tr>
<td>line width</td>
<td>75</td>
<td>75</td>
<td>100</td>
<td>100</td>
<td>75</td>
</tr>
<tr>
<td>line space</td>
<td>75</td>
<td>75</td>
<td>100</td>
<td>100</td>
<td>85</td>
</tr>
<tr>
<td>via diameter in production</td>
<td>125</td>
<td>125</td>
<td>100</td>
<td>175</td>
<td>100</td>
</tr>
<tr>
<td>max via layers</td>
<td>3×2</td>
<td>1×2</td>
<td>1×2</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>dielectric thickness</td>
<td>40–80</td>
<td>60–80</td>
<td>60</td>
<td>100–250</td>
<td>50</td>
</tr>
<tr>
<td>dielectric thickness control</td>
<td>difficult</td>
<td>good</td>
<td>good</td>
<td>good</td>
<td>good</td>
</tr>
<tr>
<td>dielectric constant</td>
<td>3.8</td>
<td>3.8</td>
<td>3.8</td>
<td>3.5</td>
<td>3.5</td>
</tr>
<tr>
<td>glass transition temperature</td>
<td>130°C</td>
<td>170°C</td>
<td>170°C</td>
<td>170°C</td>
<td>170–200°C</td>
</tr>
<tr>
<td>process issues</td>
<td>pinholes</td>
<td>conformity</td>
<td>conformity</td>
<td>via filling</td>
<td>via shape</td>
</tr>
<tr>
<td>process issues</td>
<td>adhesion</td>
<td>adhesion</td>
<td>hole cleaning</td>
<td></td>
<td></td>
</tr>
<tr>
<td>process issues</td>
<td>thickness control</td>
<td></td>
<td></td>
<td></td>
<td>non-uniform via</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>slow process</td>
</tr>
<tr>
<td>Process</td>
<td>Company</td>
<td>Material</td>
<td>Lines/Spaces</td>
<td>Via/Land</td>
<td>Via Process Diameter</td>
</tr>
<tr>
<td>----------------------------------</td>
<td>----------</td>
<td>-----------------</td>
<td>--------------------</td>
<td>------------------</td>
<td>----------------------</td>
</tr>
<tr>
<td>DV-Multi</td>
<td>NEC</td>
<td>Epoxy Film</td>
<td>80-50/80-50 μm</td>
<td>100/250 μm</td>
<td>Photo</td>
</tr>
<tr>
<td>IBSS</td>
<td>Ibiden</td>
<td>Epoxy Film</td>
<td>75-50/75-50 μm</td>
<td>150-100/250-150 μm</td>
<td>Photo</td>
</tr>
<tr>
<td>ALIVH</td>
<td>Matsushita</td>
<td>Aramid Epoxy</td>
<td>60/90</td>
<td>150/300 μm</td>
<td>Laser</td>
</tr>
<tr>
<td><strong>PERL (Plasma Etched Rdistribution Layers)</strong></td>
<td>Hewlett-Packard</td>
<td>Epoxy film PI/Aramid</td>
<td>75/50 μm and 75/50 μm</td>
<td>125-90/250-165 μm</td>
<td>Plasma/Laser</td>
</tr>
<tr>
<td>Build-up Substrate</td>
<td>Fujitsu</td>
<td>Epoxy</td>
<td>40/40 μm</td>
<td>90/140 μm</td>
<td>Photo</td>
</tr>
<tr>
<td>VB-2</td>
<td>Victor</td>
<td>Epoxy</td>
<td>10-95/100-75 μm</td>
<td>200-100/μm</td>
<td>Photo</td>
</tr>
<tr>
<td>B²IT</td>
<td>Toshiba</td>
<td>BT Laminate</td>
<td>90/90 μm</td>
<td>200/300 μm</td>
<td>Paste/Bump</td>
</tr>
<tr>
<td>Multi-Layer Build-Up</td>
<td>Shinko</td>
<td>Multiple</td>
<td>40/40 μm</td>
<td>50/110 μm</td>
<td>Laser/Photo</td>
</tr>
<tr>
<td>SLC (Surface Laminar Circuit)</td>
<td>IBM Yasu</td>
<td>Epoxy Liquid</td>
<td>75/50 μm and 125-90/250-65 μm</td>
<td>Photo via</td>
<td></td>
</tr>
<tr>
<td>Hitavia</td>
<td>Hitachi</td>
<td></td>
<td>100/100</td>
<td>200/500</td>
<td></td>
</tr>
<tr>
<td>Viathin</td>
<td>Sheldahl</td>
<td>PI</td>
<td>50/37.5 μm</td>
<td>60-25/140-75 μm &amp; 85/50/200-165 μm</td>
<td>Laser</td>
</tr>
<tr>
<td>ViaPly</td>
<td>CTS</td>
<td>PI/Aramid</td>
<td>75/75 μm</td>
<td>125/125 μm</td>
<td>Photo</td>
</tr>
<tr>
<td>TLPS</td>
<td>Ormet</td>
<td>PI</td>
<td>50/50 μm</td>
<td>25/200 μm</td>
<td>Photo</td>
</tr>
<tr>
<td>DYCOstrate</td>
<td>Dyconex</td>
<td>PI</td>
<td>100/125 μm</td>
<td>75/300 μm</td>
<td>Plasma</td>
</tr>
</tbody>
</table>
ALIVH Technology - an SBU methodology

ALIVH boards (Any Layer Interstitial (inner) Via Hole) needs no through-hole.

This is because any two layers are electrically connected by IVH (Interstitial Via Hole).

The IVH can be placed in any position.

Wiring capability is improved greatly.
Via in Pad

Plated thorough hole (PTH) is filled by epoxy resin and plated by Cu as lid. Via in Pad structure can save surface area for wiring enabling the PTH pad to be able to mount SMT devices.

Flow property of conductive epoxy or other resin crucial for minimal shrinkage and electrical contact between layers.

Minimum PTH diameter is 0.15mm, aspect ratio can be 8-10.

1. Provides a flat coplanar surface for component attachment
2. More traces on PCB escaping devices through rout channels
3. Increased component density due to absence of periphery vias
4. Potential EMI benefits due to lower inductance
5. Thermal dissipation (either at the lead joints or under devices by means of heat pipes
6. No via plugging by soldermask required at the component locations
1. Conductive Ag bumps are printed on a sheet of Cu foil.
2. Prepreg is pierced through by the bumps
3. Another sheet of Cu is also laminated and a two sided B2IT board is manufactured.

B²IT is a Toshiba Process Technology