Review

• **Types of packages**
  • DIP, QFP, PGA, BGA, CSP etc

• **Acronyms used for packages**

• **Plastic and Ceramic**
  • Materials for packages
  • Impact of materials on electrical and thermal performance

• **Application areas and cost-performance**
Materials influence performance: both electrical and thermal

Signal propagation delay influenced by the dielectric constant. (Note: speed = 1/delay)

1. Peripheral: DIP to PLCC to QFP to fine pitch QFP
2. Area array: Ceramic and plastic PGA to BGA to fine pitch BGA
3. Flip chip: Ceramic flip chip to organic flip chip

Source: “Fundamentals of MSP” – Rao Tummala
Cooling

- Package must transport heat from IC to environment
- Heat removed from package by:
  - Air: Natural air flow, forced air flow improved by mounting heat sink
  - PCB: Transported to PCB by package pins
    - Better substrates for PCB and efficient PCB design
  - Liquid: Used in large mainframe computers
The time for signals to propagate between devices, known as interconnect or resistance-capacitance (RC) delay, becomes the dominant effect and can eliminate the benefits of higher density, smaller devices. Metal resistivity and dielectric constant should be low to reduce RC delay. Therefore, Cu-lowK interconnects are preferred in packages and PWBs to improve performance. Therefore organic substrates are a better proposition. But factors like TCE, Tg, water absorption and processability limit the use of organics in high frequency applications although they are low-cost.

**Metal-glass lamination**

Hermeticity has been required for various applications over the years, and now many more packages are available with that option. It’s been difficult to produce a hermetic package that protects the electrical integrity of the chip while handling the thermal requirements and providing high reliability. However, using glass lamination and metallization has resulted in the ability to make hermetic versions of some popular existing packages.
The land grid array (LGA) is a type of surface-mount packaging for integrated circuits (ICs) that is notable for having the pins on the socket rather than the integrated circuit. An LGA can be electrically connected to a printed circuit board (PCB) either by the use of a socket or by soldering directly to the board.

Figure Source: Wikipedia Commons and AMD
PGA technology imposes limitations on the electrical and thermal capability and form-factor requirements of next-generation platforms. Land-Grid-Array (LGA) socket technology was developed as a means to avoid those limitations.

LGA is used as a physical interface for microprocessors of the Intel Pentium 4 (Prescott), Intel Xeon, Intel Core 2, Intel Core (Bloomfield and Lynnfield) and AMD Opteron families. Unlike the pin grid array (PGA) interface found on most AMD and older Intel processors, there are no pins on the chip; in place of the pins are pads of bare gold-plated copper that touch pins on the motherboard.
Ceramic Ball Grid Array (CBGA):
A ball grid array package with a ceramic substrate.

CGA - Column Grid Array
An integrated circuit package in which the input and output points are high temperature solder cylinders or columns arranged in a grid pattern.

Ceramic Column Grid Array (CCGA):
The same as CBGA except the solder balls are replaced by solder columns. The advantage of columns is that the inherent flexibility of the columns help compensate for CTE mismatch between the ceramic component and the FR-4 board. Columns are considered as an option over solder balls for components greater than 25mm square.

- High Density Interconnections
- High board reliability
- Interconnections (joints) have better solder fatigue life compared to solder balls
- High temperature solder can be used in conjunction with ceramic substrate
- Higher stand-off distance with the base substrate
- Flexible yet stress free connection with the bond pad of the substrate
Some Basic Package Physical Parameters..

<table>
<thead>
<tr>
<th>Substrate Material</th>
<th>FR4 / BT</th>
<th>Ceramic</th>
<th>Polymer</th>
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<tr>
<th>Die-attach</th>
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<th>Leads</th>
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Figure Source: Dr Arun Chandrasekhar, Intel, India.
### Physical Parameters of a PGA Package

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#### PIN GRID ARRAY

- Plastic-BT or FR4
- Stacked
- Flip Chip/WB
- Solder Balls
- Overmold
PCB Layer Construction

CROSS SECTION

HDI-Layer

HDI-Layer

CORE

4

3

2

1

Die

organic
substrates

Fan-out
I/O's

via

BGA

Figure Source: IPC Designers Council
Staggered Micro Vias
Stacked Micro Vias

Figure Source: IPC Designers Council
**BGA Packages**

- No. of I/O pins and device density are increasing
- Continuous push towards miniaturization at lower costs
- High pin count and fine-pitch BGAs
- BGA provides increased functionality at the same package size as QFPs
- BGA improves ratio of pin count to board size
- BGA balls are stronger than QFP leads- can be handled better
- BGA offers reduced package thickness compared to leaded components
- BGA offers better electrical and thermal performance by providing ground plane for a low-impedance power system
- BGA routing is a key factor in board design
The CTE mismatch between silicon die and organic substrate is the main reason for failure in microelectronics packages.

In order to increase the reliability it is better to:
- increase the package size
- increase the interconnect (solder ball in a BGA) size
- design the interconnects outside the die area (partial array)
- But these changes will increase the package size and decrease the performance
- With bare die on board, an underfill can be used to nullify thermal effects (underfills are epoxy based media with filler added to get required CTE)

Figure Source: Joseph Fjelstad, Tessera
Lead-free solder balls used in BGA packages

Figure Source: CEDT, IISc
BGA interconnects can be repaired

Figure Source: CEDT, IISc
BGA interconnects can be repaired

BGA sockets are available for test purposes only.
BGA is best used by direct soldering on to substrate.

Figure Source: CEDT, IISc
3D Packaging - Stacked Die

- **Definition:** Packaging Technology with 2 or More DIE
  - Stacked in a Single Package or Multiple Packages Stacked Together

- **Supports**
  - Wirebond Die Attach
  - Flip chip Die Attach
  - Hybrid - Combination of Flip-Chip and Wirebond

- **Packaging Applications**
  - CSP
  - BGA
  - Folded over package (PoP)

- **Benefits of 3D Packaging**
  - Smaller, Thinner and Lighter Packages
  - Reduced Packaging Costs and Components
  - System Level Size Reduction Due to Smaller Footprints and Decrease Component Count (SiP)

- Common for Wireless Handsets, Handheld Electronics and Memory Intensive Requirements.

*Figure Source: Wikimedia Commons ( sketch)*
Multi Chip Modules (MCM) or Multi chip packaging

- Industry’s first MCM from IBM.
- Generally MCMs are horizontal or two-dimensional modules.

Defined as a single unit containing two or more chips and an interconnection substrate which function together as a system building block.

Need for MCM
- More functionality in one ‘single chip’
- Special circuit needs met
- MCMs formed from multiple chips on a common substrate / package structure
- Do away with individually packaged chips on a PWB

Figure Source: Prof Rao R Tummala, PRC, GTech.
Multiple Chip Module (MCM)

- Increase integration level of system (smaller size)
- Decrease loading of external signals, hence, higher electrical performance
- No packaging of individual chips
- Problems with cooling; special cooling requirements may be required yet
- Still expensive; but used for high-end applications (e.g., military, aerospace etc); a complete PC in a MCM possible