REVIEW OF THE TOPICS SO FAR

- Levels of packaging
- Definition of product, system
  - Case studies of systems packaging
- Roadmaps
- Semiconductor wafer fab process
- First level connection choices
- Packages
  - Package form factors
  - Package suitable for 2nd level interconnection
PACKAGES

SINGLE CHIP PACKAGES OR SINGLE CHIP MODULES

MULTICHIcip PACKAGES OR MULTI CHIP MODULES
What is a Single chip package?

A single chip package is a package that supports a single microelectronic device so that its electrical, mechanical, thermal and chemical performance are adequately served.

The device originates from a wafer, gets singulated or diced, then packaged and burnt-in and tested. Such a packaged IC may contain millions of transistors or integrated circuits.

An example is the PGA format packages seen in Intel’s microprocessors for personal computers.
Functions of single chip packages

1. Provide an efficient means for signal transmission and power distribution to and from the IC with which it is packaged.
2. Provide an efficient means for signal transmission and power distribution between the packaged device and other components of the system through subsequent assembly onto a system board.
3. Enable the device to be attached to the next level of packaging through a suitable interconnect scheme such as surface mount technology, SMT.
4. Allow for effective dissipation of heat generated by the packaged device during its operation.
5. Provide adequate protection of the device from external forces of mechanical or environmental nature which may damage the device.
6. Act as space transformer between the fine pitch grid of IC that is typically in the 100 micron range and the PWB grid that is typically in the 200 micron range.
Types of Single Chip Packages:

- IC Package Materials
  - Plastic
  - Thin Film (Tape carrier)
  - Ceramic
- IC Assembly
  - SMT (Surface Mount Technology)
  - PTH (Pin-Through-hole or Plated-through-hole)
  - DCA (Direct Chip Attach)
- IC Interconnection
  - Peripheral (Quad Flat Pack)
  - Partial Area Array
  - Area Array (Ball Grid Array)
Historical evolution of single chip packages. (Courtesy of Motorola)

Source: “Fundamentals of MSP” – Rao Tummala
IC packaging efficiency of various single chip packages.

Source: “Fundamentals of MSP” – Rao Tummala
Power distribution with minimum noise and electromigration
• Better signal integrity
  • Lead-free solder bumping possible
  • Nano interconnections
  • MEMS and MoEMS fabricated interconnects
• Integrates wafer fab, packaging, test and burn-in at wafer level

WLP is essentially a true CSP technology
No single industry standard exists at present
Perennial Debate on wires and bumps!
A Chip is Useless without a Package

• Delivers power to the Chip efficiently

• Transfers information into and out of the Chip to the PCB
  – Space transformer

• Draws heat away from the Chip

• Protects the Chip from outside elements
Chip Package is a space transformer for chip to PCB interconnection.

Electrical, mechanical, thermal, material issues

Source: “Fundamentals of MSP” – Rao Tummala
IC Packages

- Molding Compounds
- Wirebond
- Leadframe
- Die Attach Adhesive
- Pin
- Package
- Pad
- Cavity
Why Package ICs?

Pure silicon die is difficult to handle
- Die is very fragile
- Die is very small

IC package is some sort of mechanical interface of the die and it’s environment
- Prevent from damages during
  - Manufacturing (i.e. soldering)
  - Normal use
Why Package ICs?

IC package prevents the die from electrical stress
- EMC
- UV light
  - EEPROM
- X-rays
  - Space conditions, avionic environment
Packaging Requirements

Speed
- Short chip-to-chip propagation delays
- High bandwidth

Pin count and wireability
- Large IO count per chip edge
- Dense wiring

Size
- Compact size to reduce board space
Packaging Requirements

- Thermal and mechanical
  - High heat removal rate
  - Good match between thermal expansion coefficients of the dice and the chip carrier
  - Prevent the die from destruction

- Test, reliability, cost
  - Easy to manufacture, test, modify and fix
  - Highly reliable
  - Low cost
Chip mounting

• Pin through hole
  – Pins traversing PCB
  – Easy manual mounting
  – Problem passing signals between pins on PCB (All layers)
  – Limited density

• Surface Mount Devices (SMD)
  – Small footprint on surface of PCB
  – Special machines required for mounting
  – No blocking of wires on lower PCB layers
  – High density

(QFN for example)
## Types of single chip packages

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Material</th>
<th>Pin Count (Total I/O)</th>
<th>Min. Pitch (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Through-Hole</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single In Line (SIP)</td>
<td>Plastic</td>
<td>&lt; 48</td>
<td>1.27</td>
</tr>
<tr>
<td>Dual In Line (DIP)</td>
<td>Plastic (PDIP)</td>
<td>&lt; 84</td>
<td>2.54</td>
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<tr>
<td></td>
<td>Ceramic (CDIP)</td>
<td>&lt; 84</td>
<td>2.54</td>
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<tr>
<td><strong>Surface Mount</strong></td>
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<td></td>
<td></td>
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<tr>
<td>Small Outline (SO)</td>
<td>Plastic (SOP/J)</td>
<td>&lt; 84</td>
<td>1.27</td>
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<tr>
<td>Leaded Chip Carrier (LCC)</td>
<td>Plastic (PLCC)</td>
<td>&lt; 120</td>
<td>1.27</td>
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<tr>
<td>Quad Flat Pack (QFP)</td>
<td>Plastic (PQFP)</td>
<td>&lt; 356</td>
<td>0.30</td>
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<tr>
<td></td>
<td>Ceramic (CQFP)</td>
<td>&lt; 356</td>
<td></td>
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<tr>
<td>Tape Automated Bonding</td>
<td>Plastic (TAB)</td>
<td>&lt; 356</td>
<td>0.25</td>
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<td><strong>Area Array</strong></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Pin Grid Array (PGA)</td>
<td>Plastic (PPGA)</td>
<td>&lt; 750</td>
<td>1.27</td>
</tr>
<tr>
<td></td>
<td>Ceramic (CPGA)</td>
<td>&lt; 750</td>
<td>1.27</td>
</tr>
<tr>
<td>Ball Grid Array (BGA)</td>
<td>Plastic (PBGA)</td>
<td>&lt; 800</td>
<td>1.00</td>
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<tr>
<td></td>
<td>Plastic (FC-PBGA)</td>
<td>&lt; 1700</td>
<td>1.00</td>
</tr>
<tr>
<td></td>
<td>Ceramic (FC-CBGA)</td>
<td>&lt; 800</td>
<td>1.00</td>
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<tr>
<td>Column Grid Array (CGA)</td>
<td>Ceramic (FC-CBGA)</td>
<td>&lt; 1700</td>
<td>1.00</td>
</tr>
<tr>
<td>Chip Scale Package (CSP)</td>
<td>Plastic (CSP, μBGA)</td>
<td>&lt; 356</td>
<td>0.50</td>
</tr>
<tr>
<td></td>
<td>Ceramic (CSP)</td>
<td>&lt; 356</td>
<td>0.50</td>
</tr>
</tbody>
</table>

**Notes:**
- 14-DIP refers to a specific type of Through-Hole package.
- The min. pitch values for Through-Hole packages are indicated in red.