Review

Front-end processing
- Sand to Silicon (purity)
- Silicon to Wafer (Silicon)
  - Sizes (dia) Thickness
- Clean Room
  - 32 nm
  - 22 nm
  - 11 nm
- Wafer Ingot Slicing

Wafer Die

Photoresist (PR)
- Types
  - UV Exposure (photolithography)
    - Mask

Developing
- PR Stripper

Etching - Types
- Wet etch
- DRY etch

Deposition
- Self-implanting

TESTING
Test, Assembly & Packaging: Back-end

Materials management, Chemical Distribution, Automation, CIM

- Wafer Test
- Dicing — INDIVIDUAL DIE
- Die Bond — Substrate?
- Wire Bond — first-level interconnection methodology
- Encapsulation — Protects (Molding)
- Test & Burn-In
Encapsulation and Decoupling
Packaging
The substrate, the die and the heat spreader are put together to form a completed processor. The green substrate builds the electrical and mechanical interface for the processor to interact with the rest of the PC system. The silver heat spreader is a thermal interface where a cooling solution will be put on to. This will keep the processor cool during operation.

Source: INTEL
Processor
Completed processor (Intel® Core™ i7 Processor in this case). A microprocessor is the most complex manufactured product on earth. In fact, it takes hundreds of steps –only the most important ones have been visualized in this picture story -in the world's cleanest environment (a microprocessor fab) to make microprocessors.

Source: INTEL
Class Testing
During this final test the processors will be tested for their key characteristics (among the tested characteristics are power dissipation and maximum frequency).
Binning
Based on the test result of class testing processors with the same capabilities are put into the same transporting trays.

Source: INTEL
Retail Package
The readily manufactured and tested processors (again Intel® Core™ i7 Processor is shown here) either go to system manufacturers in trays or into retail stores in a box such as that shown here.

Source: INTEL
You can also visit the following websites for very informative videos on semiconductor manufacturing:

www.siliconrun.com

www.nec.com
PACKAGING EVOLUTION HAS BEEN SLOWER COMPARED TO SEMICONDUCTOR EVOLUTION

Time and Packaging Efficiency

Source: Wikimedia Commons
Peripheral to Area Array: Another Packaging Example to increase density

Picture Source: NASA
Small Form Factor: A Packaging Example with QFPs
Example

<table>
<thead>
<tr>
<th>Type</th>
<th>Area</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>QFP</td>
<td>900 mm²</td>
<td>100%</td>
</tr>
<tr>
<td>TAB</td>
<td>400 mm²</td>
<td>44%</td>
</tr>
<tr>
<td>Chip-on-Board</td>
<td></td>
<td></td>
</tr>
<tr>
<td>COB</td>
<td>225 mm²</td>
<td>25%</td>
</tr>
<tr>
<td>CSP</td>
<td>115 mm²</td>
<td>13%</td>
</tr>
<tr>
<td>Flip Chip</td>
<td>100 mm²</td>
<td>11%</td>
</tr>
</tbody>
</table>

Wafer-level packaging as the future trend.

From QFP to flip chip:

Savings in real estate and increase in density, performance
SOC, SIP & SOP: Complementary

**SOC:**
- Multi-functions in one chip around digital cores

**SIP:**
- Stacked ICs with the diverse functions

**SOP:**
- Single system package with multiple functions embedded in die and package as thin films

**Source:** TI and Prof Rao Tummala, GTech
Chip level interconnections

- 1\textsuperscript{st} level interconnection
  - Connection of die to the package
    (single or multichip; SCM or MCM)

- 2\textsuperscript{nd} level interconnection
  - Connection of the package to the PWB
Package-to-Board Interconnect

(a) Through-Hole Mounting

- Plated through hole Technology (PTH or THT)
  - Leaded components require through hole

(b) Surface Mount

- Surface Mount Technology (SMT)
  - Leaded components mounted on surface
  - Direct chip attach like flip chip (DCA)
  - Chip on Board (COB) using wirebonding
  - Solder ball based connection like BGA, CSP
Common 1\textsuperscript{st} level interconnections

\rightarrow 1. Wire bonding
\rightarrow 2. Tape automated bonding
\rightarrow 3. Flip chip bonding
Two options:
- Ball bonding
- Wedge bonding

Two options:
- Face up chip
- Face down chip

Three options:
- Metallurgical bond
- Metallurgical and adhesive bond
- Adhesive bond
Chip to package connection

- **Wire bonding**
  - Only periphery of chip available for IO connections
  - Mechanical bonding of one pin at a time (sequential)
  - Cooling from back of chip
  - High inductance (~1nH)

Picture Source: Palomar Technologies
Wirebond Attachment

- Used in Lead Frame, PGA and BGA packaging
- Over 80% of Packages are Wire bonded
- Epoxy Glue to Attach Chip
- Typically Gold Wire
  - Also Copper, Aluminum
  - Wire length- typ. 1-5 mm
  - Wire diam.- typ. 25-35 μm
  - Inexpensive, Reliable

- Molding or Encapsulation done with epoxy resin
- Chip-on-Board involves glob top to bare die with epoxy resin