IC
Die
- KGD - Known Good Die
- Chip
- Singulated die
- Active device
- Wafer
- Wafer fab (fabrication)

PCB (PWB)
- Printed Circuit Board
  - Printed Wiring Board
  - Printed Circuit Board Assembly (PCBA)

Types
- 2nd level package
  - Organic (plastic)
  - Inorganic (ceramic)

First level packaging
CHAPTER/MODULE 2:
SEMICONDUCTOR FABRICATION AND PACKAGING
Fabrication overview: Front-end

Materials management, Chemical Distribution, Automation, CIM

- Mask preparation
  - Wafer manufacturing
  - Epitaxy
    - Homoepitaxy, Heteroepitaxy / pure
    - Photolithography
  - Photoresist Application
  - Etch and Strip
  - Diffusion/ Implant Dopants: P, B, k, Cu, As, etc...
  - CMP- Chemical Mechanical Planarization
  - Inspection, Test and Measurement

Clean Room

VLST CAD

Silicon (Si)
Test, Assembly & Packaging: Back-end

Materials management, Automation, CIM

- Wafer Test
- Dicing (Singulate)
- Die Bond (KGD/Substrate)
- Wire Bond (Au, Al, Cu; First level interconnect: Bond pads/Die → headframes of the package)
- Encapsulation (Protection; Molding Process)
- Test & Burn-In (Thermal Cycling)
Some Basics

- Semiconductor has resistivity lying between that of conductor and insulator.
- It establishes its conduction properties through a complex quantum mechanical behaviour within a periodic array of semiconductor atoms.
- The resistivity is proportional to the free carrier density and this can be changed widely by doping different atomic species.
- Some dopants establish electron carrier density (n-type) and some establish hole carrier density (p-type).
- Electric fields enable electric switching between a conducting state and a non-conducting state. (carrier transport)
- Group IV elements: Ge, Si, C and Sn;
- Si is the most commonly used because of its abundance on earth.
Formation of Semiconductor crystals

Bonding arrangements of atoms in semiconductor crystals. (a) Elemental semiconductor such as silicon. (b) Compound III-V semiconductor such as GaAs. (c) Compound II-VI semiconductor such as CdSe.
Everything starts with sand...

Metallurgical-Grade Silicon (MG-Si)

$$\text{SiO}_2 + 2C \rightarrow 2000^\circ C \rightarrow \text{Si} + 2\text{CO}$$

Purity: 97% but we need: 99.9999%

Eleven Nines Purity of Si

Fabrication

Si - Ingot → Si - Wafers → Wafer Processing → Oxidation, Masking/Patterning, Etching → Wire Bonding → Encapsulated IC

Processed wafer → Die Attach → Wire Bonding → Encapsulated IC

Manufacturing: A Lithographic Process

Photographic glass plate (mask)

Each layer is projected to the silicon die

Source: Peter Nilsson, LTH, Sweden
**Clean Room classifications**

- Class 1: $1 \text{/cm}^3 = 70.5 \mu\text{m}$
- Class 10: $10 \text{/ft}^3$
- Class 100: 100
- Class 1000: 1000
- Class 10,000: 10,000

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**Wafer Stepper**

- Light goes through the mask, lens, and the objective

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**Clean Room**

- **Clothing**
  - particles in the air
    - Air in a city: 15 million - 100 million particles per ft$^3$
    - Air in the mountains: up to 10 million particles per ft$^3$
    - Air in a clean room for ICs: 1 - 100 particles per ft$^3$
Electron mobility of semiconductors is used to describe the relation between the drift velocity of electrons or holes in a solid material or electrons/ions in a gas in an applied electric field.

*Unit cm²/V.s*

Strongly dependent on impurities and dopants. The conductivity of the semiconductor is dependent on the mobility of the dominant charge carrier.

Typical electron mobility of
- GaAs at 300K is ≈9000 cm²/V.s
- Si at 300K is ≈1400
- Ge at 300K is ≈4000
Making the Wafer

• A seed crystal is suspended in a molten bath of silicon

• It is slowly pulled up and grows into an ingot of silicon

• The ingot is removed and ground down to diameter

• The end is cut off, then thin silicon wafers are sawn off (sliced) and polished

• For example, in a 8” wafer about 500 devices/chips can be accommodated by design. They are rectangular in shape

• Wafers are processed typically in batches of 25 (lot)
1. Chip = Die = Microchip = Bar
2. Scribe Lines
3. Engineering Test Die
4. Edge Die
5. Crystal Planes
6. Wafer Flats

Source: Institute of Microelectronic Systems
Wafers have flats, and the flats told you two things:

The doping type of the wafer (n- or p-type)

The orientation of the wafer: \{100\} or \{111\}
Wafer processing
   Wet cleans
   Photolithography
   Ion implantation (in which dopants are embedded in the wafer creating regions of increased (or decreased) conductivity)
   Dry etching
   Wet etching
   Plasma ashing
   Thermal treatments
      Rapid thermal anneal
      Furnace anneals
      Thermal oxidation
   Chemical vapor deposition (CVD)
   Physical vapor deposition (PVD)
   Molecular beam epitaxy (MBE)
   Electrochemical Deposition (ECD). See Electroplating
   Chemical-mechanical planarization (CMP) (Polishing)
   Wafer testing (where the electrical performance is verified)
   Wafer backgrinding (to reduce the thickness of the wafer so the resulting chip can be put into a thin device like a smartcard or PCMCIA card.)

Plastic or ceramic packaging involves mounting the die, connecting the die pads to the pins on the package, and sealing the die. Tiny wires are used to connect pads to the pins. In the old days, wires were attached by hand, but now purpose-built machines perform the task. Traditionally, the wires to the chips were gold, leading to a “lead frame” (pronounced “leed frame”) of copper, that had been plated with solder, a mixture of tin and lead. Lead is poisonous, so lead-free “lead frames” are now mandated by ROHS.
## Semiconductor manufacturing processes

<table>
<thead>
<tr>
<th>Feature</th>
<th>Year</th>
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<tr>
<td>10 μm</td>
<td>1971</td>
</tr>
<tr>
<td>3 μm</td>
<td>1975</td>
</tr>
<tr>
<td>1.5 μm</td>
<td>1982</td>
</tr>
<tr>
<td>1 μm</td>
<td>1985</td>
</tr>
<tr>
<td>800 nm (0.80 μm)</td>
<td>1989</td>
</tr>
<tr>
<td>600 nm (0.60 μm)</td>
<td>1994</td>
</tr>
<tr>
<td>350 nm (0.35 μm)</td>
<td>1995</td>
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<tr>
<td>250 nm (0.25 μm)</td>
<td>1998</td>
</tr>
<tr>
<td>180 nm (0.18 μm)</td>
<td>1999</td>
</tr>
<tr>
<td>130 nm (0.13 μm)</td>
<td>2000</td>
</tr>
<tr>
<td>90 nm</td>
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<td>22 nm</td>
<td>approx. 2011</td>
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<tr>
<td>16 nm</td>
<td>approx. 2013</td>
</tr>
<tr>
<td>11 nm</td>
<td>approx. 2015</td>
</tr>
</tbody>
</table>

Wafer sizes are 300mm, 450mm

Source: Web
From Sand to Silicon to Wafer…. is an interesting process.

Now, you will see a short video clip titled Sand-to-Silicon. This video is reproduced with written permission from Intel.