CHAPTER ONE

A general overview of electronics packaging

Content will include:
Electronic systems and needs. Physical integration of circuits, packages, boards and full electronic systems. System applications like computer, automobile, medical and consumer electronics with case studies. Packaging levels.
Essentials of every electronic product or system

- Semiconductor devices such as ICs
- Packaging to integrate these ICs and other devices into components
- System-level boards which integrate these components to form the system-level assemblies that provide all functions required of the system.
  - Functions are typically electrical such as analog and digital
  - Components must provide the needed mechanical and chemical functions
  - Systems packaging involves electrical, mechanical and materials technologies
CHIP LEVEL PACKAGING

Design

Environment

Materials

Reliability

Board Assembly

Test

Manufacturing

SYSTEM LEVEL PACKAGING

BOARD LEVEL PACKAGING

Fig courtesy: Lord Corporation
Why is Microelectronics Systems Packaging important?

• Every IC and Device has to be packaged
• Controls performance of computers
• Controls size of consumer electronics
• Controls reliability of electronics
• Controls cost of electronic products
• Required in nearly every industry such as automotive, communications, computer, consumer, medical, aerospace and military.
Chapter 1 Objectives:

To appreciate the importance and role of packaging (electrical and thermal), material, manufacturing and reliability issues in the design and manufacturing of electronic products.

Learning Objectives:

- Understand the nature of electronic industry and its evolution
- Understand the structure of an electronic product
Learning Objectives ...

- Appreciate the role and evolution of ICs
- Understand the role of packaging
- Appreciate different issues of packaging
- Identify all the manufacturing technologies
- Appreciate system level issues in different areas of application
To Support the Industry Growth:

- Next-Generation System Technologies
- Skilled Human Resources
  - Globally-Competitive, System-Level Engineers with Complete Product Development Education

2009-10

Electronics > $ 3.0T
Microelectronics & Packaging > $ 500B
Electronics Packaging > $ 220B
Indian Electronic Industry (2008-09) ~ $ 20B
IC Revenues $307 Bn

silicon value $260 Bn

IC Packaging and Functional Test $47 Bn

Through hole package $0.45Bn

Array Package $22.1 Bn

Surface Mount Package $24.4 Bn

BGA/PGA $16.8 Bn

CSP $5.3 Bn
INDIA-CHINA ELECTRONICS HARDWARE PRODUCTION

(Various sectors of electronics)
Electronic industry is characterized by

- Technology driving the business
- Rapid technological advances
- Continuous price erosion
- High growth rates
- Large volumes and global markets
- Short life cycles
Technologies of concern

- Silicon
- Packaging
- Magnetic storage
- Display
- Optical ,RF
- Sensor, MEMS and MoEMS
- Material and Nano-materials
- Software-embedded
Audion (Triode), 1906
Lee De Forest

First point contact transistor (germanium), 1947
John Bardeen and Walter Brattain
Bell Laboratories
First integrated circuit (germanium), 1958
Jack S. Kilby, Texas Instruments

Contained five components, three types:
Transistors, resistors and capacitors

Intel Pentium II, 1997
Clock: 233MHz
Number of transistors: 7.5 M

Figure reproduced from: www.texasingenuity.com
Figure reproduced from: Intel from web and tayloredge.com
History

- 1971 Microprocessor invented
  - Intel produces the first 4-bit microprocessor the 4004
  - The 4004 was a 3 chip set
    - 2 kbit ROM IC
    - 320 bit RAM IC
    - 4-bit processor
    - Each housed in a 16- pin DIP package
  - Processor:
    - 10 mm silicon gate PMOS process
    - ~2300 transistors
    - Clock speed: 0.108 MHz
    - Die size: 13.5 mm²

Figure reproduced from: Intel from web and tayloredge.com
Source: Intel
History

- 1982 Intel 80286
  - 1.5 mm silicon gate CMOS process
  - 1 polysilicon layer
  - 2 metal layers
  - 134,000 transistors
  - 6 to 12 MHz clock speed
  - Die size 68.7 mm²
History

- **2000 Pentium 4**
  - 0.18 mm silicon gate CMOS process
  - 1 polysilicon layer
  - 6 metal layers
  - Fabrication: 21 mask layers
  - 42,000,000 transistors
  - 1,400 to 1,500 MHz clock speed
  - Die size 224 mm²

Figure reproduced from: Intel from web and tayloredge.com

Product of Intel
Current Technology

2005 - Intel Pentium 4TM (65nm)
Intel introduced a 65nm process in 2005. The single poly-silicon CMOS process has 8 layers of copper metal and requires an estimated 31 mask layers. The 65nm Pentium 4 has 169 million transistors and the die size is 189.9 mm2. Intel soon switched to the new smaller "Core" design.

2007 - Intel Core 2 Duo (45nm)
Intel's 45nm debuted in 2007 as the first high-k gate oxide with dual metal gates in production. The 45nm process is a single poly-silicon process with 9 copper layers and requires and estimated 36 mask layers. The 45nm Core 2 Duo die size is 105.78mm2 and packs in 410 million transistors.
The wafer is separated into chips by a diamond grindstone. A fully automatic dicing saw is used for dicing.

The separated IC chip (die) is bonded into the center of a lead frame or package.

The pads on the IC chip and adjoining terminals on the lead frame are connected, one-by-one, with gold wire.

The chip is sealed with a macro-molecule plastic, like epoxy resin, thus finishing the plastic package container.

The lead frame is cut, and leads are bent thus forming the package. The manufacturer's name and model number are stamped on top.
“Moore’s Law”

- In 1965 Gordon Moore (then at Fairchild Corporation) noted that:
  - Number of components per chip doubles approx. every 18 months
  - This statement is commonly known as “Moore’s Law”
  - It has proven to be “correct” till this day
  - “Integration complexity doubles every three years”

What is behind this fantastic pace of development of the IC technologies?
- Is it the “technological” will and motivation of the people involved?
- Or/and is it the economical drive the main force?

Semiconductor industry sales:
- 1962, > $1-billion
- 1978, > $10-billion
- 1994, > $100-billion
- 2007, > $2.5-3T
### ITRS Roadmap for Semiconductors (2008 summary)

**DRAM ½ PITCH Flash Memory (nm)**

<table>
<thead>
<tr>
<th>Year</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
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<tr>
<td>Pitch</td>
<td>68</td>
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<td>52</td>
<td>45</td>
<td>40</td>
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</table>

The common measure of the technology generation of a chip.

**CHIP SIZE DRAM (mm²)**

<table>
<thead>
<tr>
<th>Year</th>
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<th>2008</th>
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<td>93</td>
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**DRAM ½ PITCH High performance microprocessor (nm)**

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<tr>
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<td>59</td>
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<td>36</td>
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# ITRS Roadmap for Semiconductors (2008 summary)

## Package Pins

<table>
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<tr>
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<tr>
<td>600-21</td>
<td>600-21</td>
<td>660-28</td>
<td>660-27</td>
<td>720-30</td>
<td>720-33</td>
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<td>40</td>
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<td>01</td>
<td>83</td>
<td>61</td>
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## Power supply voltage (high performance)

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<td>1.1</td>
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<td>1.0</td>
<td>1.0</td>
<td>0.95</td>
<td>0.90</td>
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</table>

## Maximum Power (Watts) (high-performance with heat sink)

<table>
<thead>
<tr>
<th></th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
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<td>146</td>
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<td>161</td>
<td>158</td>
<td>149</td>
<td></td>
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</tbody>
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**Source**

International Technology Roadmap for Semiconductors
Driving force: Economics

- Traditionally, the cost/function in an IC is reduced by 25% to 30% a year.
  - This allows the electronics market to grow at 15% / year

- To achieve this, the number of functions/IC has to be increased. This demands for:
  - Increase of the transistors count
    - increased functionality
  - Increase of the clock speed
    - more operations per unit time = increased functionality
  - Decrease of the feature size
    - contains the area increase = contains price
    - improves performance
Driving force: Economics

❖ Increase productivity:
  ➢ Increase equipment throughput
  ➢ Increase manufacturing yields
  ➢ Increase the number of chips on a wafer:
    • reduce the area of the chip:
      - smaller feature size & redesign
  ➢ Use the largest wafer size available (300, 450mm?)

  “Is there a limit?”

  Much depends on equipment manufacturers
Industry Statistics

- What is the approximate cost of setting up a wafer fab?
- High volume factory:
  - Total capacity: 40K Wafer Starts Per Month (WSPM) (180nm)
  - Total capital cost: $2.7B
    - Production equipment: 80%
    - Facilities: 15%
    - Materials, handling systems: 3%
    - Factory information & control: 2%
Industry Statistics...

- Worldwide semiconductor market (chip market) revenues in 2010: ~$310.3B (up by 35% from 2009)
  - Semiconductor market growth rate
    - ~15% / year
  - Equipment market growth rate:
    - ~19.4% / year
  - By 2011 equipment spending will exceed 30% of the semiconductor market revenues
<table>
<thead>
<tr>
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<tbody>
<tr>
<td><strong>Low Cost</strong></td>
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<td></td>
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<tr>
<td>Cost (Cents/pin)</td>
<td>0.34-0.77</td>
<td>0.29-0.66</td>
<td>0.25-0.57</td>
<td>0.22-0.49</td>
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<tr>
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<td>125</td>
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<tr>
<td><strong>High Performance</strong></td>
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<td></td>
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<tr>
<td>Cost (Cents/pin)</td>
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<td>170</td>
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<tr>
<td>Performance (MHz)</td>
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<td>1000</td>
<td>1250</td>
<td>1500</td>
<td>1800</td>
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**PACKAGING ROADMAP**
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<td><strong>Single-chip Package Technology Requirements</strong></td>
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<td>*Low-cost/hand held</td>
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<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
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<tr>
<td>*Cost-performance</td>
<td>140</td>
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<td>804</td>
<td>750</td>
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<tr>
<td>*Harsh</td>
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<td>100</td>
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<td><strong>Maximum Power (W/mm²)</strong></td>
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<td>*Harsh</td>
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<td><strong>Core Voltage (V)</strong></td>
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<tr>
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<tr>
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<td>160-850</td>
<td>170-900</td>
<td>180-950</td>
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<td>198-1050</td>
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</table>

Data from: International Technology Roadmap for Semiconductors
Challenges in Packaging for the industry- Roadmap topics

- Process Integration
  - Both front end and back end processes
- Device scaling
- Electrical issues- signal integrity; RF and analog/mixed
- Photolithography- bigger challenge to Moore’s law
- Masks and light source for patterning
- New materials- high conductivity and low dielectric permittivity
Challenges in Packaging for the industry-Roadmap topics...

- Manufacturability of the interconnect structures
- Power management for different applications
- Testing complexity
- Equipment challenges (very important!!)
- Manufacturing cost and cycle time
- Performance requirement of the market
- Assembly and packaging
- Resource conservation; environmental concerns
Challenges in Packaging for the industry-Roadmap topics...

- Yield enhancement for industry; large volume production
- Thermo-mechanical; Design for Reliability

Challenges are more when the industry progresses towards 22nm technology DRAM pitch. Today production is available for 65nm; designs being tested for 45nm by very few companies. It is expected to be 22nm by 2015 (short term goal) and 11nm by 2022 (long term goal).