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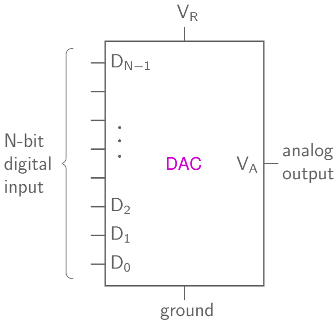
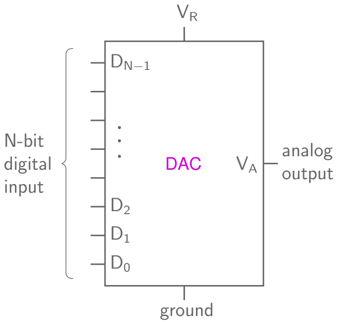
DAC

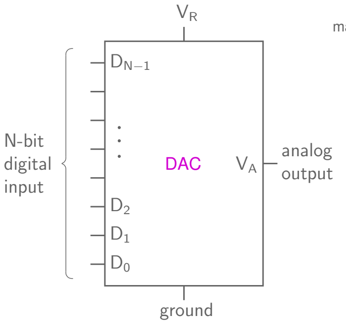


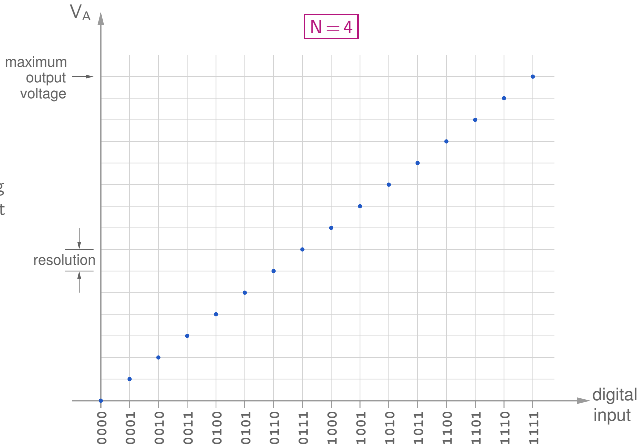
V_R
D_{N-1}
N-bit
digital
input
DAC
V_A
analog
output
D_2
D_1
D_0
ground



* For a 4-bit DAC, with input $S_3 S_2 S_1 S_0$, the output voltage is
$V_A = K\left[(S_3 \times 2^3) + (S_2 \times 2^2) + (S_1 \times 2^1) + (S_0 \times 2^0)\right]$.
In general, $V_A = K \sum_0^{N-1} S_k 2^k$.

DAC





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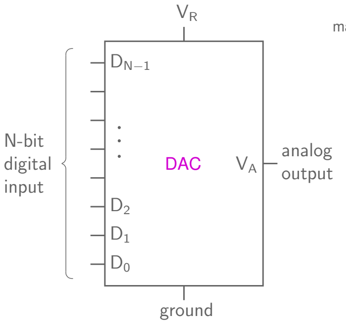

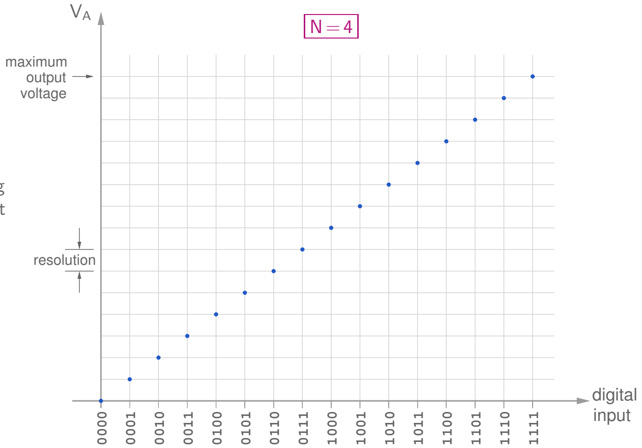

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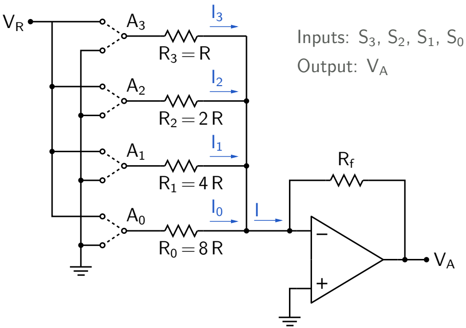
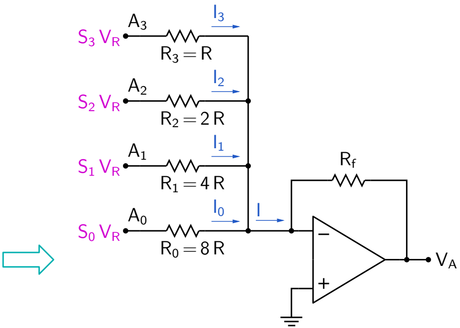
  In general, $V_A = K \sum_0^{N-1} S_k 2^k$.
* K is proportional to the reference voltage V_R. Its value depends on how the DAC is implemented.

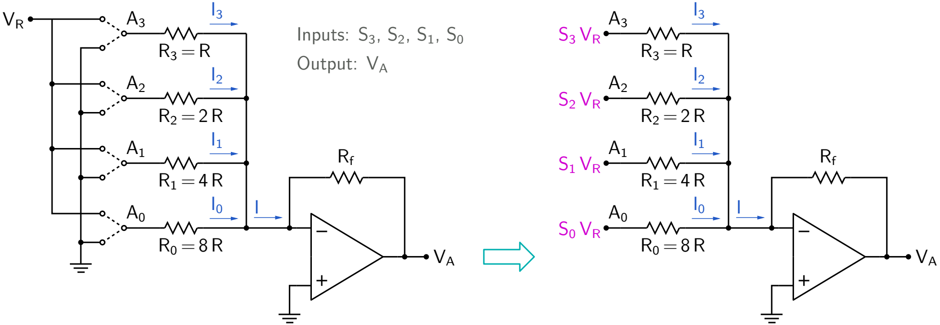
DAC using binary-weighted resistors

Inputs: S_3, S_2, S_1, S_0

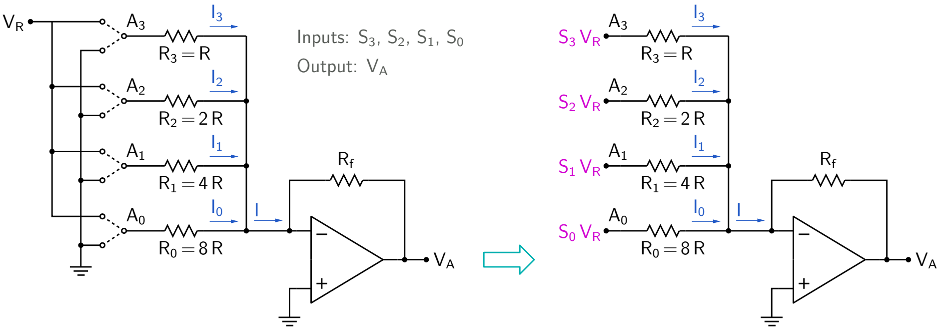
Output: V_A







* If the input bit S_k is 1, A_k gets connected to V_R; else, it gets connected to ground.



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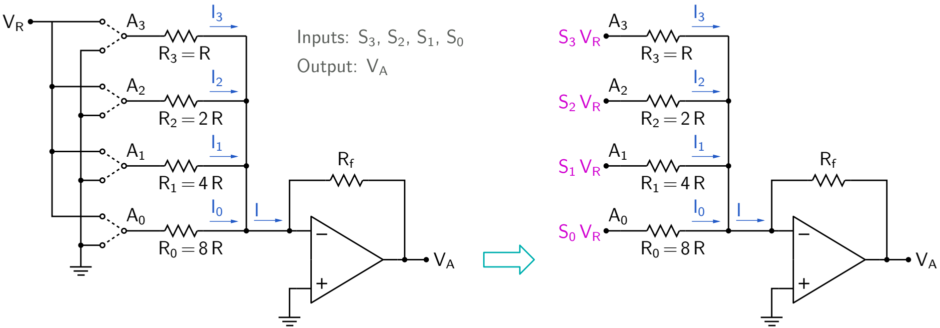
DAC using binary-weighted resistors



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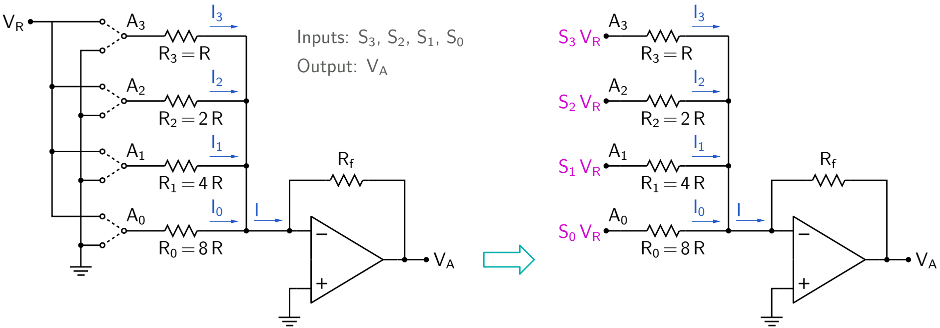

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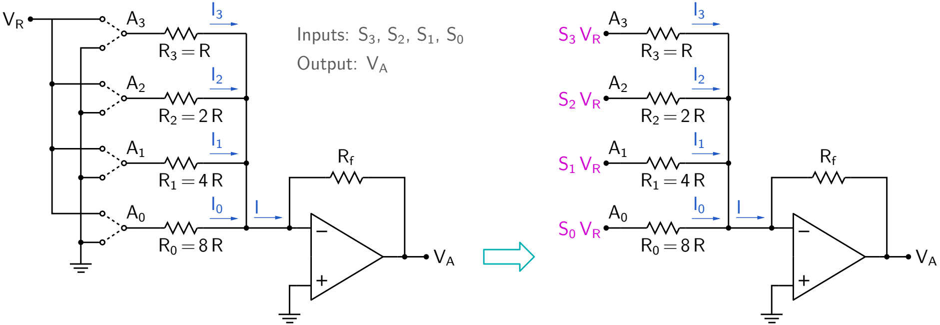
M. B. Patil, IIT Bombay

DAC using binary-weighted resistors



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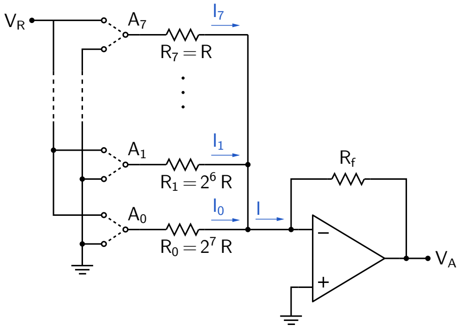
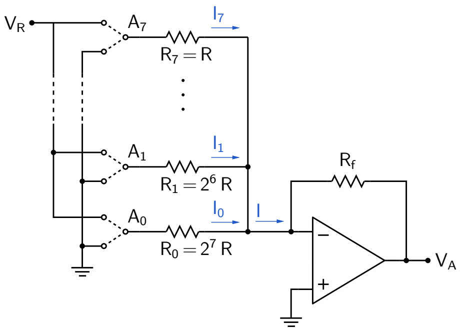
* The output voltage is $V_o = -R_f\, I = -V_R \dfrac{R_f}{2^{N-1} R} \sum_0^{N-1} S_k \times 2^k$.

DAC using binary-weighted resistors: Example





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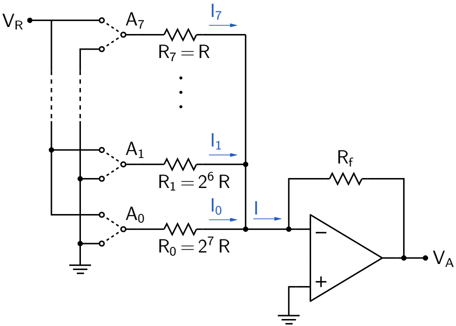

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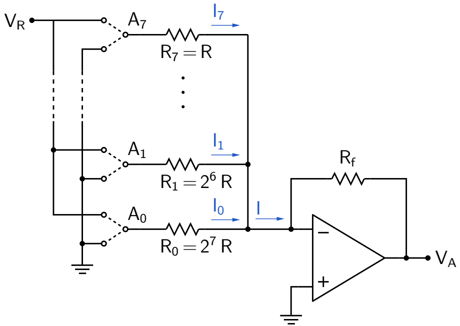

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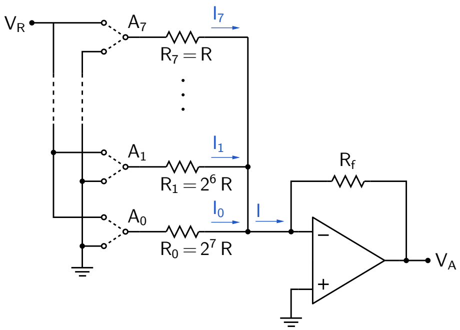

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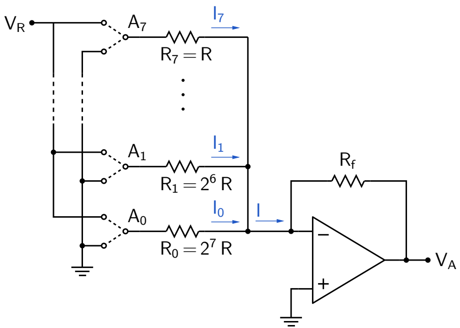

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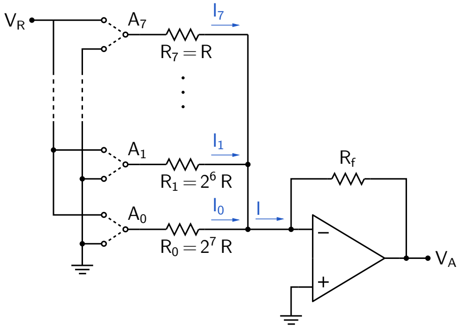
(Ref.: K. Gopalan, *Introduction to Digital Microelectronic Circuits*, Tata McGraw-Hill, New Delhi, 1978)

DAC using binary-weighted resistors: Example (from Gopalan)



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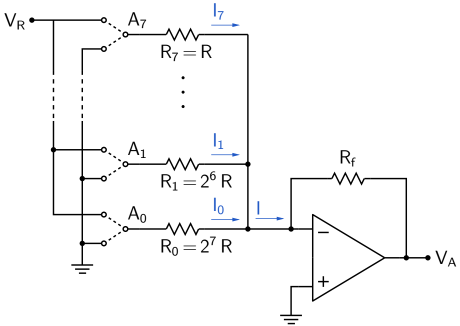

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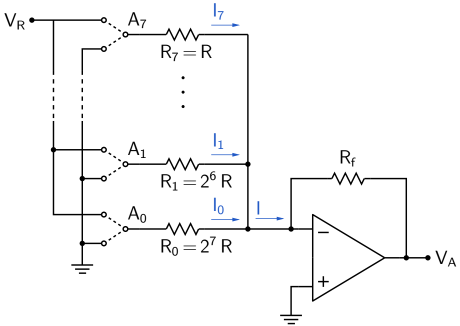

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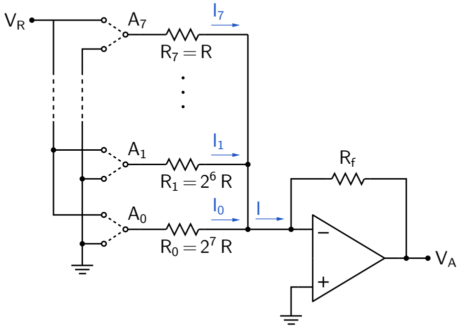

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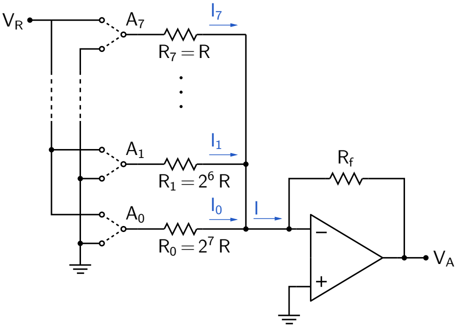
$$\rightarrow \Delta V_A = \frac{V_R}{2^{N-1}} \frac{R_f}{R} = \frac{5\,\text{V}}{2^{8-1}} \times 1 = \frac{5}{128} = 0.0391\,\text{V}.$$

DAC using binary-weighted resistors: Example (from Gopalan)



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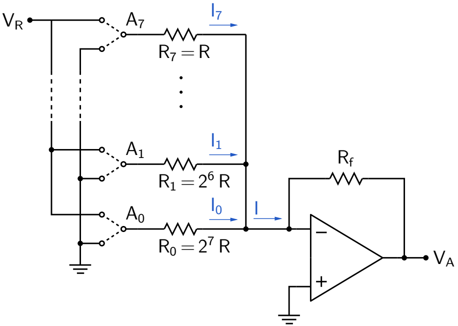

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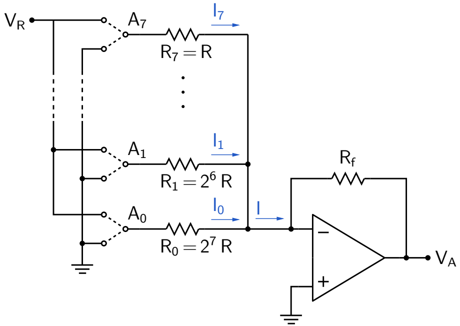

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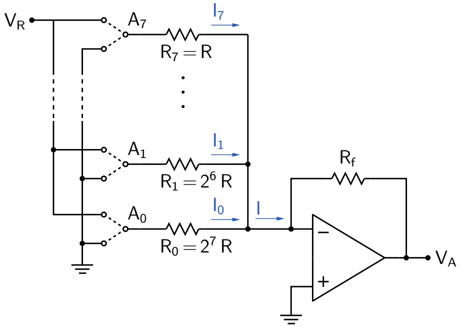

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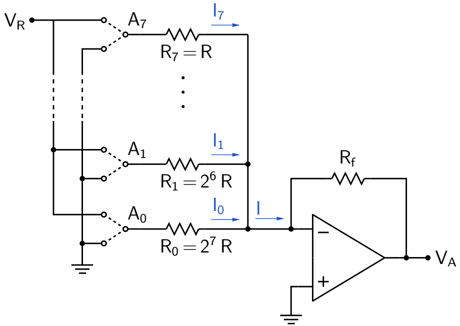

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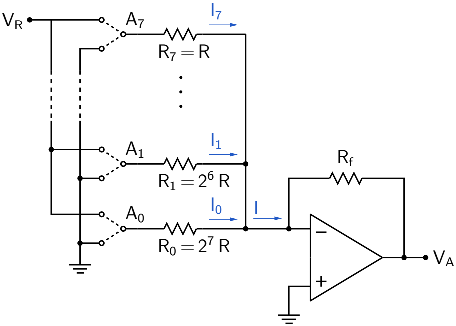
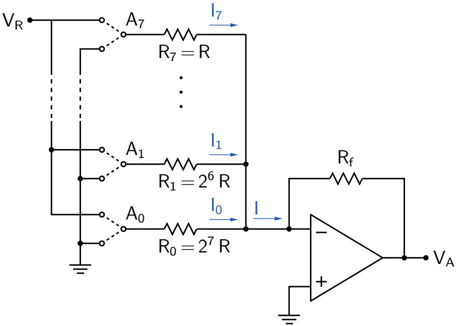
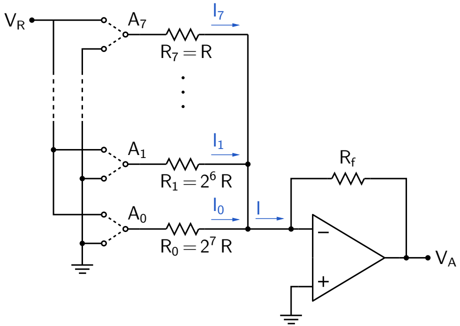
$$|V_A|^{\text{max}} = \frac{5}{128} \times 1 \times \left[2^0 + 2^1 + \cdots + 2^7\right] = \frac{5}{128} \times \left(2^8 - 1\right) = 5 \times \frac{255}{128} = 9.961\,\text{V}.$$


V_R
A_7
I_7
$R_7 = R$
A_1
I_1
$R_1 = 2^6\,R$
A_0
I_0
$R_0 = 2^7\,R$
I
R_f
V_A



* Find the output voltage corresponding to the input 1010 1101.



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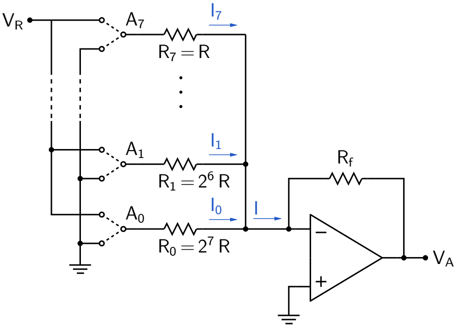

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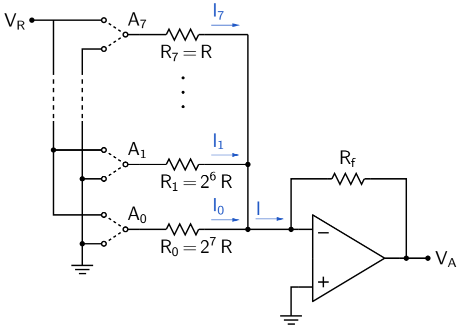
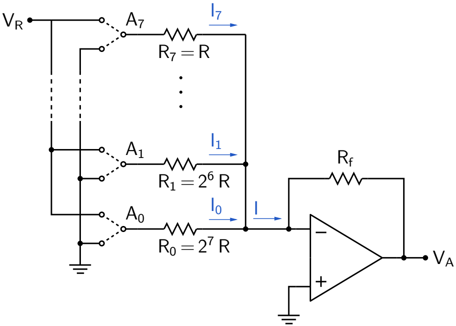
$$= -\frac{5}{128} \times 1 \times \left[2^7 + 2^5 + 2^3 + 2^2 + 2^0\right] = -5 \times \frac{173}{128} = -6.758\,\mathrm{V}\,.$$

DAC using binary-weighted resistors: Example (from Gopalan)





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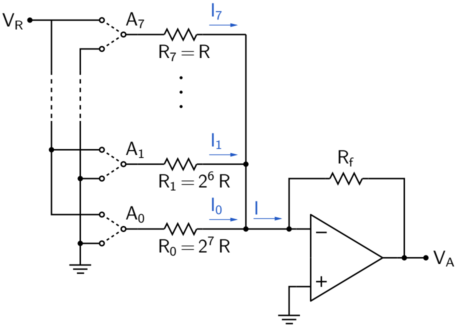

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  $|V_A|$ is maximum when (a) currents I_0, I_1, etc. assume their maximum values, with $R_k = R_k^0 \times (1 - 0.01)$ and (b) R_f is maximum, $R_f = R_f^0 \times (1 + 0.01)$.
  (The superscript '0' denotes nominal value.)

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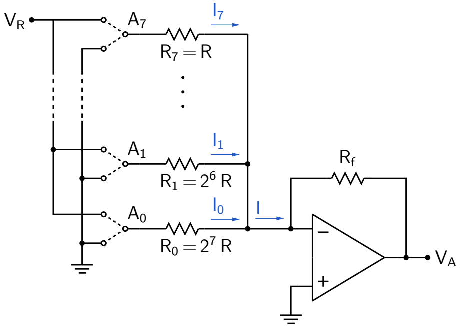

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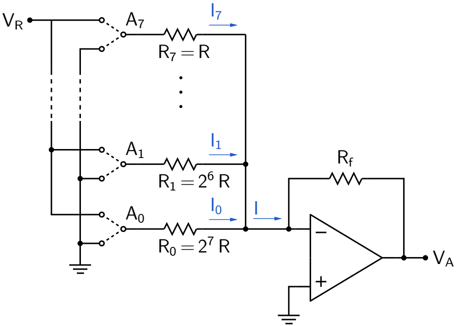
  $$\rightarrow |V_A|^{\text{max}}_{11111111} = V_R \times \frac{255}{128} \times \left.\frac{R_f}{R}\right|^{\text{max}} = 5 \times \frac{255}{128} \times \frac{1.01}{0.99} = 10.162\,\text{V}.$$



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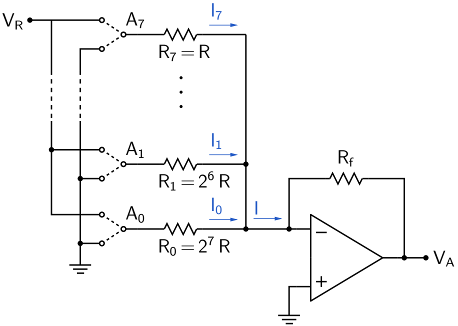
  Similarly, $|V_A|_{11111111}^{\text{min}} = 5 \times \dfrac{255}{128} \times \dfrac{0.99}{1.01} = 9.764\,\text{V}.$


V_R
A_7
I_7
$R_7 = R$
A_1
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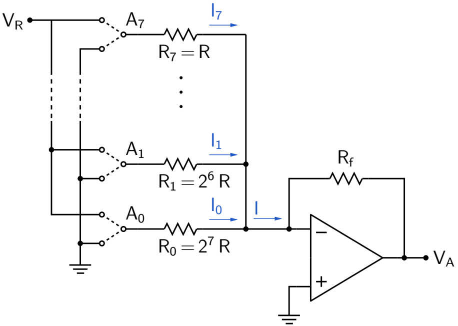
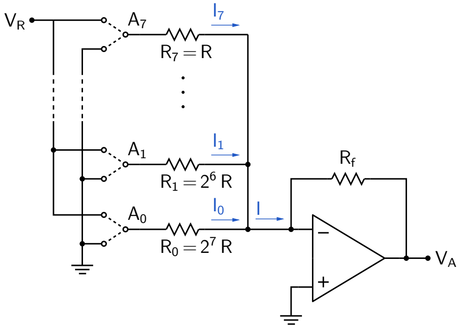
A_0
I_0
$R_0 = 2^7\,R$
I
R_f
V_A

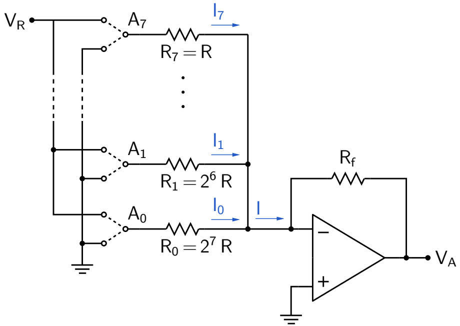
DAC using binary-weighted resistors: Example (from Gopalan)



* ΔV_A for input 1111 1111 $= 10.162 - 9.764 \approx 0.4\,\text{V}$ which is larger than the resolution (0.039 V) of the DAC. This situation is not acceptable.

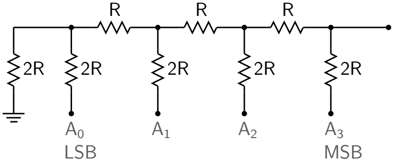


* ΔV_A for input 1111 1111 $= 10.162 - 9.764 \approx 0.4\,\text{V}$ which is larger than the resolution (0.039 V) of the DAC. This situation is not acceptable.
* The output voltage variation can be reduced by using resistors with a smaller tolerance. However, it is difficult to fabricate an IC with widely varying resistance values (from R to $2^{N-1}R$) and each with a small enough tolerance.

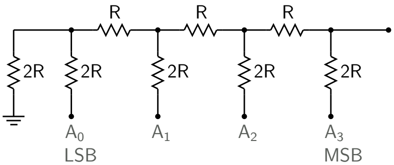


* ΔV_A for input 1111 1111 $= 10.162 - 9.764 \approx 0.4\,\text{V}$ which is larger than the resolution (0.039 V) of the DAC. This situation is not acceptable.
* The output voltage variation can be reduced by using resistors with a smaller tolerance. However, it is difficult to fabricate an IC with widely varying resistance values (from R to $2^{N-1}R$) and each with a small enough tolerance.
  $\rightarrow$ use $R - 2R$ ladder network instead.

R-2R ladder network

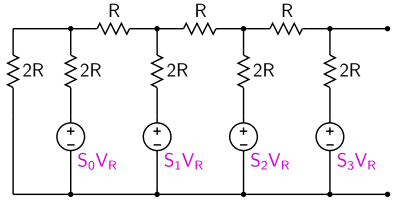


Node A_k is connected to V_R if input bit S_k is 1; else, it is connected to ground.

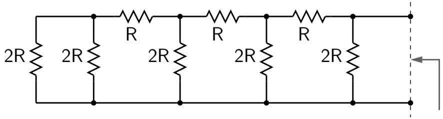


Node A_k is connected to V_R if input bit S_k is 1; else, it is connected to ground.

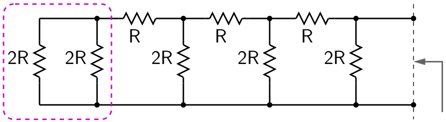
The original network is equivalent to



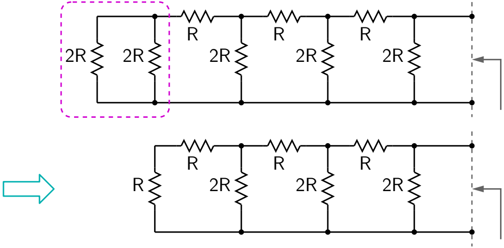
R-2R ladder network: Thevenin resistance



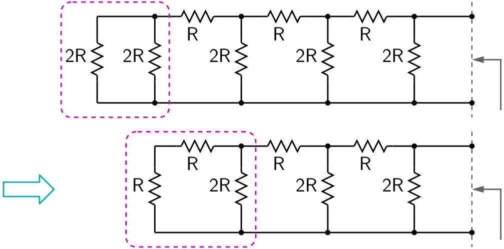
R-2R ladder network: Thevenin resistance



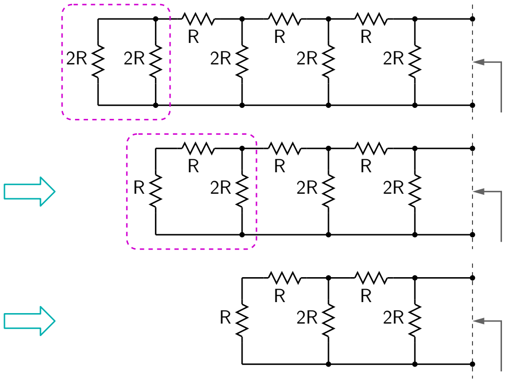
R-2R ladder network: Thevenin resistance



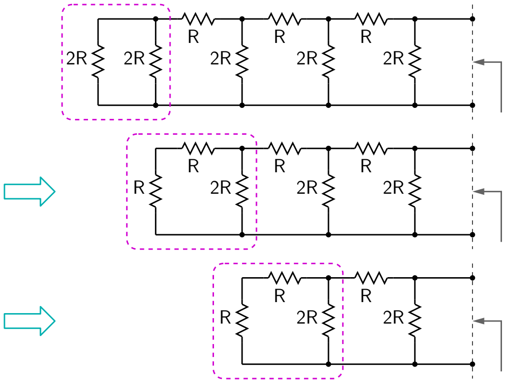
R-2R ladder network: Thevenin resistance



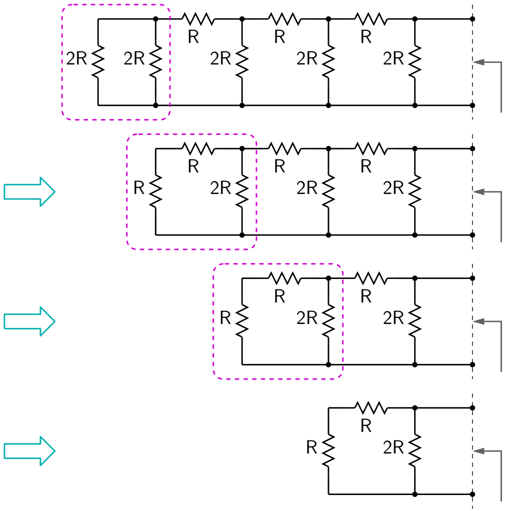
R-2R ladder network: Thevenin resistance



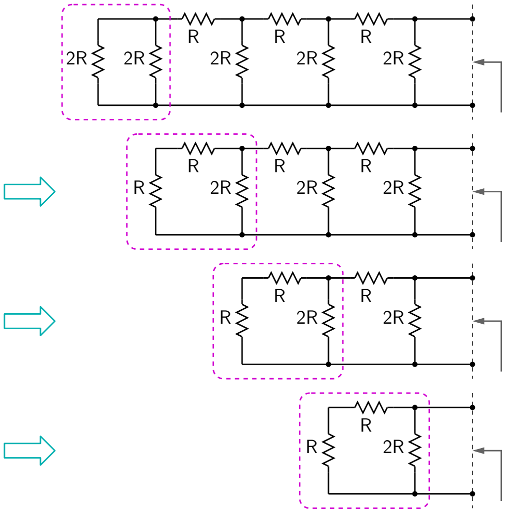
R-2R ladder network: Thevenin resistance



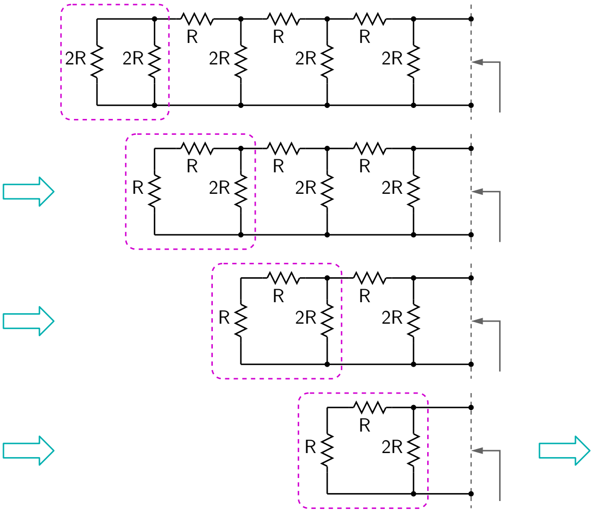
R-2R ladder network: Thevenin resistance



R-2R ladder network: Thevenin resistance

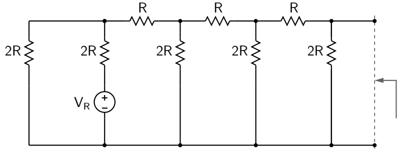


R-2R ladder network: Thevenin resistance

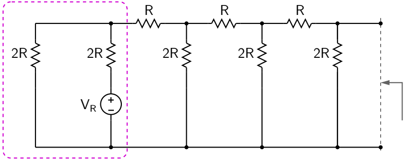


$\boxed{R_{Th} = R}$

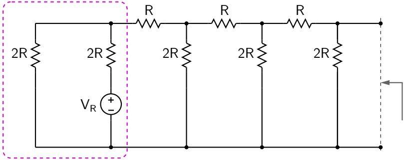
R-2R ladder network:
V_{Th} for $S_0 = 1$

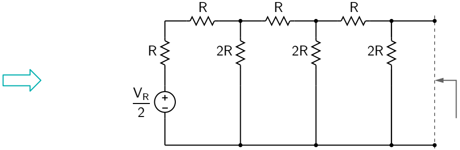


R-2R ladder network:
V_{Th} for $S_0 = 1$

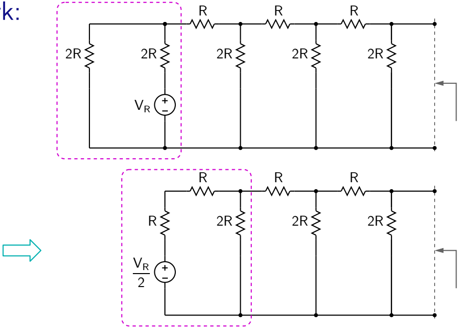


R-2R ladder network: V_{Th} for $S_0 = 1$

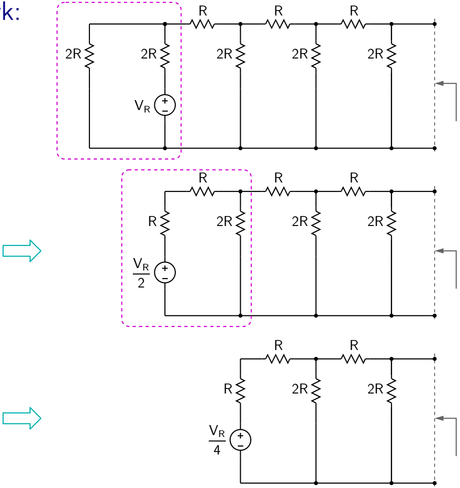




R-2R ladder network:
V_{Th} for $S_0 = 1$

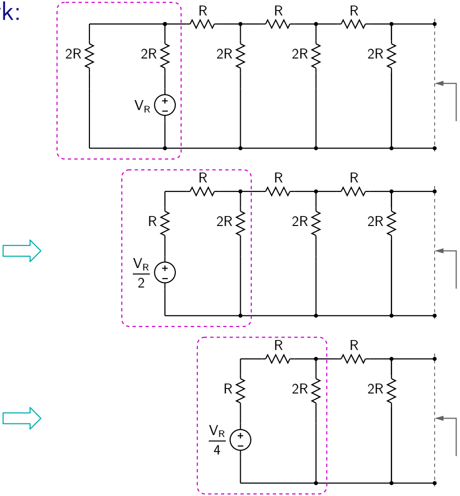


R-2R ladder network:
V_{Th} for $S_0 = 1$

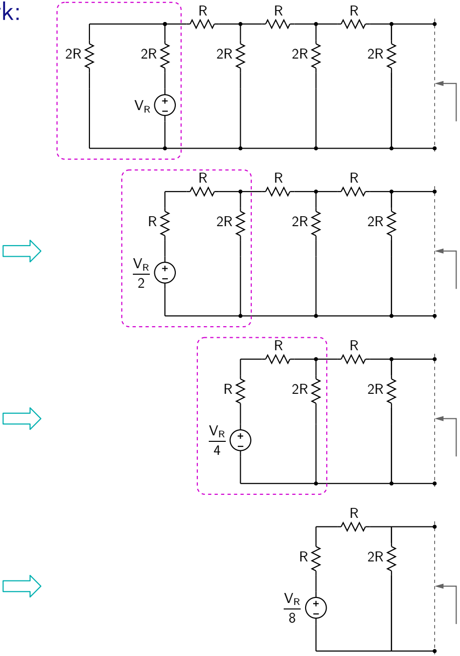


R-2R ladder network:

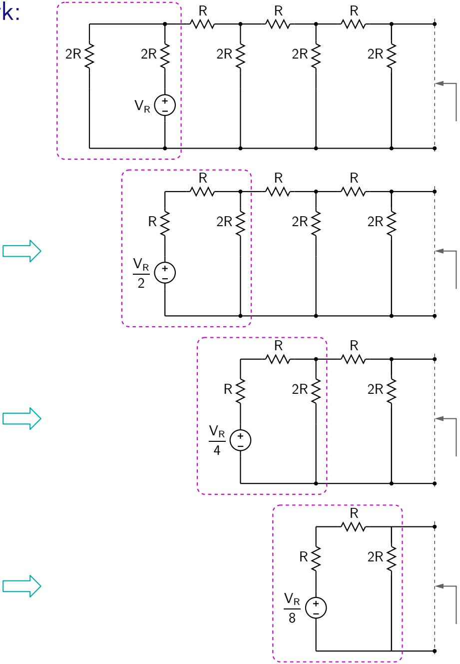
V_{Th} for $S_0 = 1$



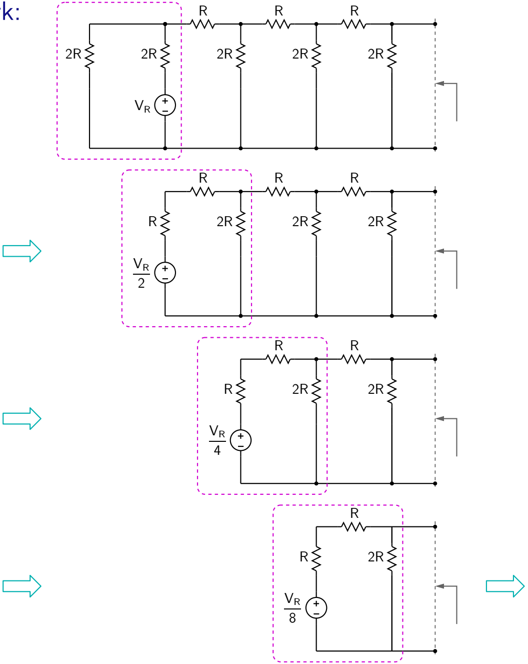
R-2R ladder network:
V_{Th} for $S_0 = 1$



R-2R ladder network:
V_{Th} for $S_0 = 1$

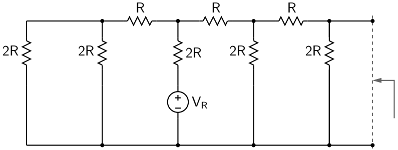


R-2R ladder network:
V_{Th} for $S_0 = 1$

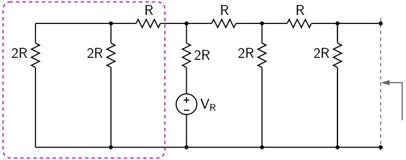


$$V_{Th} = \frac{V_R}{16}$$

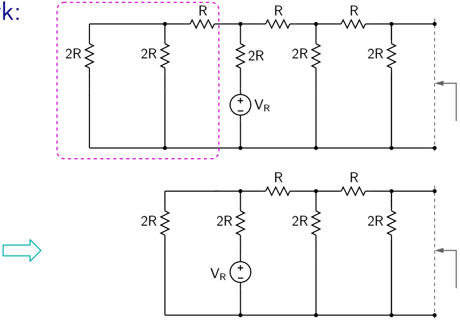
R-2R ladder network:
V_{Th} for $S_1 = 1$



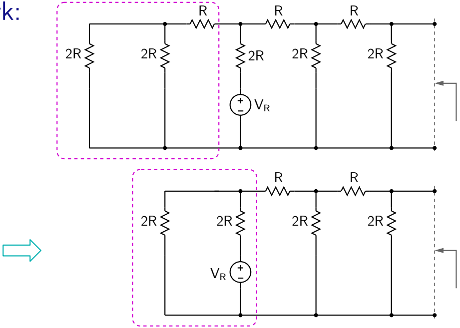
R-2R ladder network:
V_{Th} for $S_1 = 1$



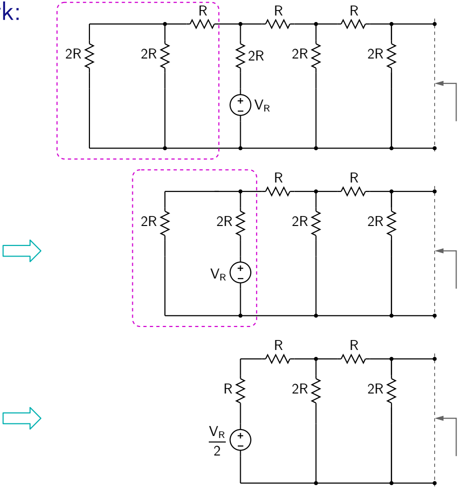
R-2R ladder network:
V_{Th} for $S_1 = 1$



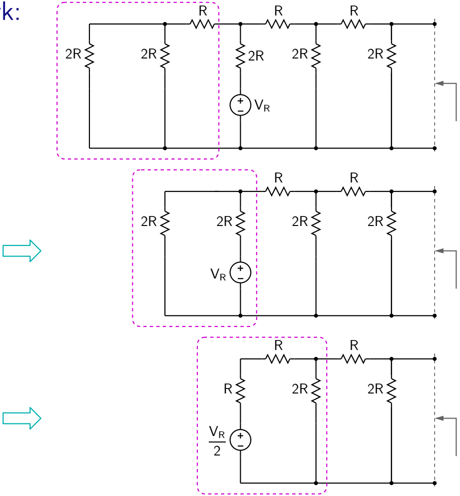
R-2R ladder network: V_{Th} for $S_1 = 1$



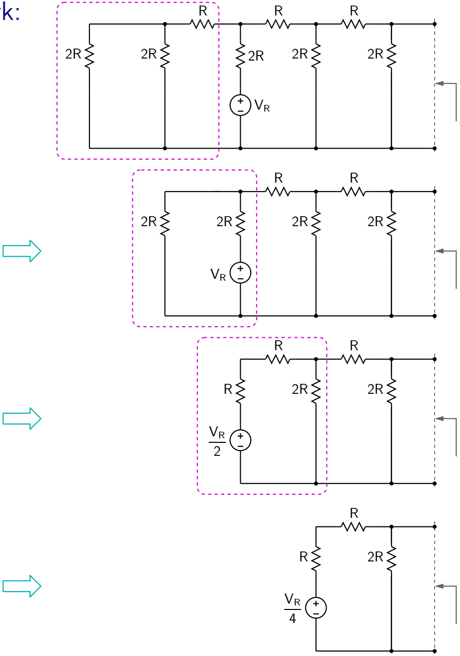
R-2R ladder network:
V_{Th} for $S_1 = 1$



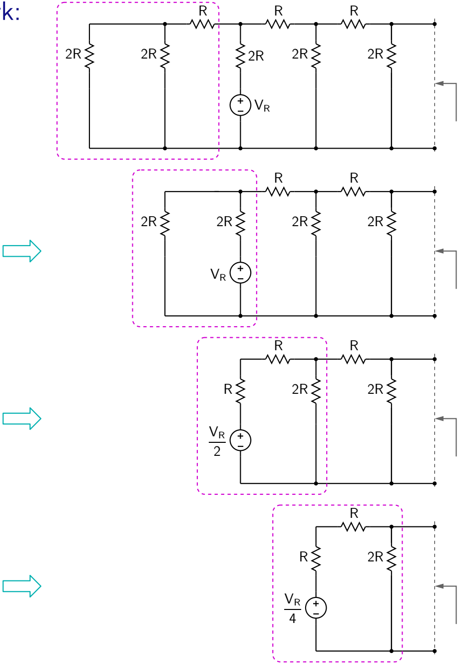
R-2R ladder network:
V_{Th} for $S_1 = 1$



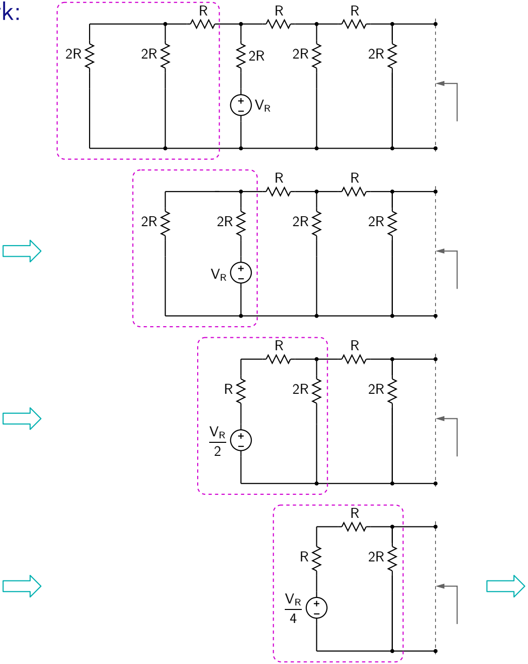
R-2R ladder network: V_{Th} for $S_1 = 1$



R-2R ladder network:
V_{Th} for $S_1 = 1$



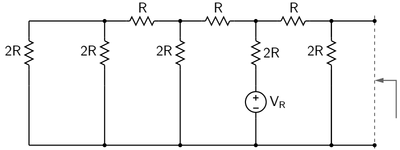
R-2R ladder network:
V_{Th} for $S_1 = 1$



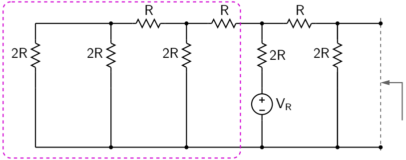
$$\boxed{V_{Th} = \frac{V_R}{8}}$$

R-2R ladder network:

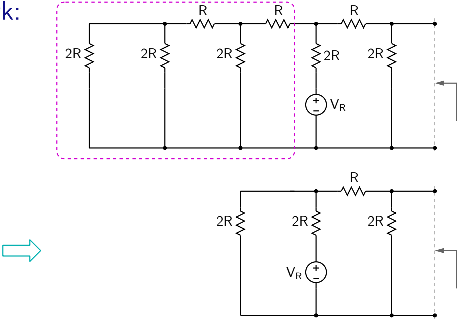
V_{Th} for $S_2 = 1$



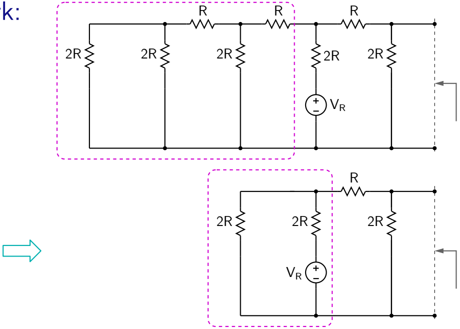
R-2R ladder network:
V_{Th} for $S_2 = 1$



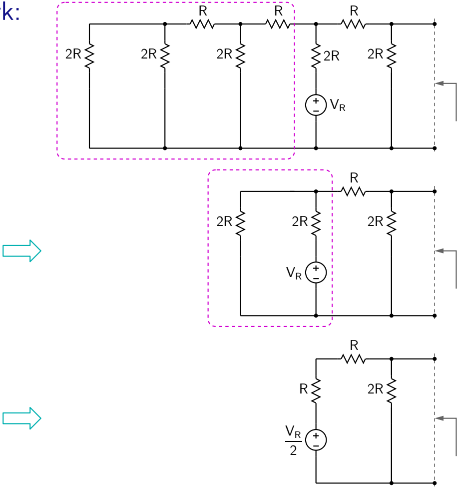
R-2R ladder network:
V_{Th} for $S_2 = 1$



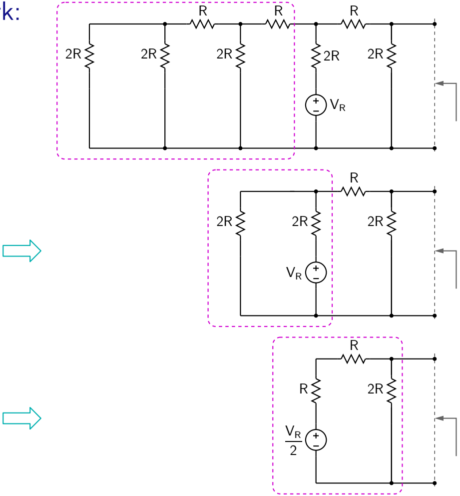
R-2R ladder network:
V_{Th} for $S_2 = 1$



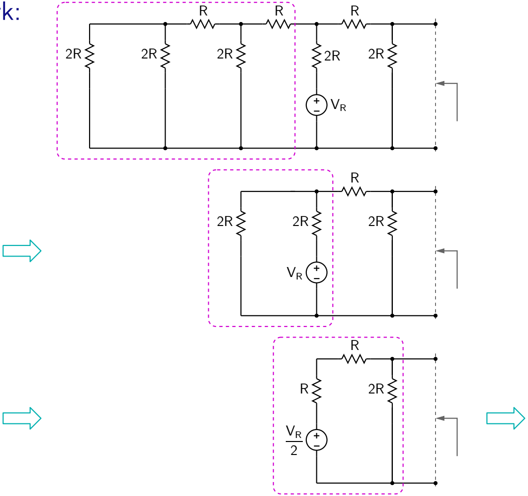
R-2R ladder network:
V_{Th} for $S_2 = 1$



R-2R ladder network:
V_{Th} for $S_2 = 1$



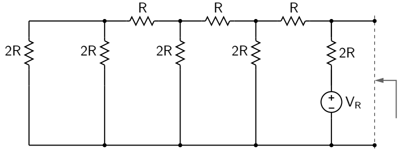
R-2R ladder network:
V_{Th} for $S_2 = 1$



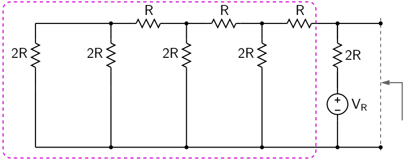
$$V_{Th} = \frac{V_R}{4}$$

R-2R ladder network:

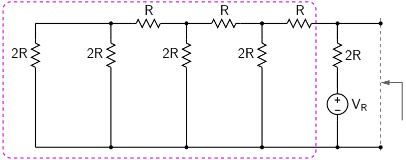
V_{Th} for $S_3 = 1$

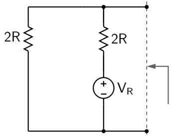


R-2R ladder network:
V_{Th} for $S_3 = 1$

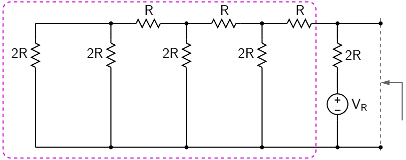


R-2R ladder network:
V_{Th} for $S_3 = 1$

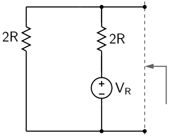




R-2R ladder network:
V_{Th} for $S_3 = 1$



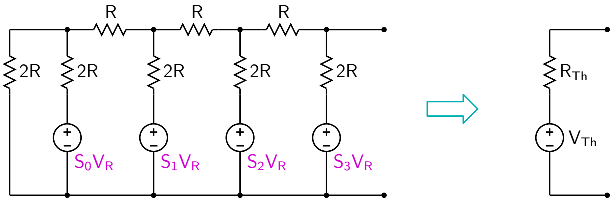
⇨



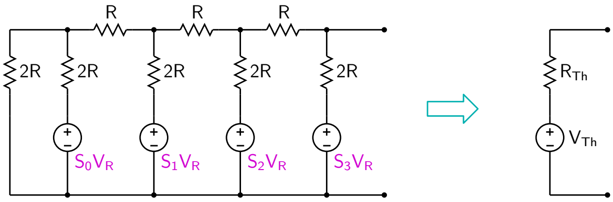
⇨

$$\boxed{V_{Th} = \frac{V_R}{2}}$$

R-2R ladder network: R_{Th} and V_{Th}

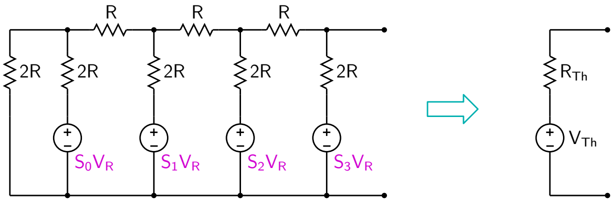


R-2R ladder network: R_{Th} and V_{Th}



* $R_{Th} = R$.

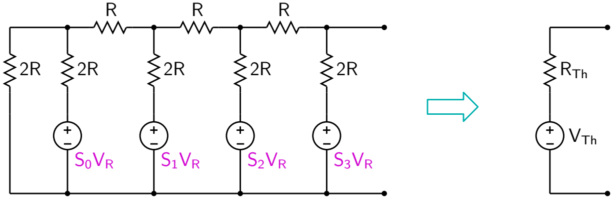
R-2R ladder network: R_{Th} and V_{Th}



* $R_{Th} = R$.
* $V_{Th} = V_{Th}^{(S0)} + V_{Th}^{(S1)} + V_{Th}^{(S2)} + V_{Th}^{(S3)}$

$$= \frac{V_R}{16} \left[S_0\, 2^0 + S_1\, 2^1 + S_2\, 2^2 + S_3\, 2^3 \right] .$$

R-2R ladder network: R_{Th} and V_{Th}

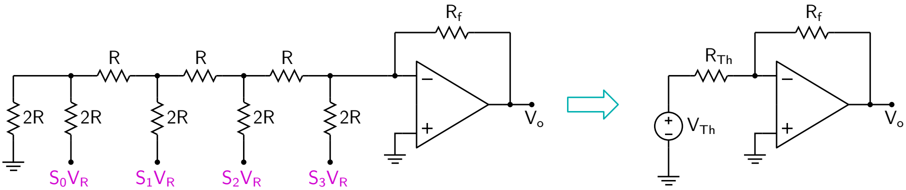


* $R_{Th} = R$.
* $V_{Th} = V_{Th}^{(S0)} + V_{Th}^{(S1)} + V_{Th}^{(S2)} + V_{Th}^{(S3)}$

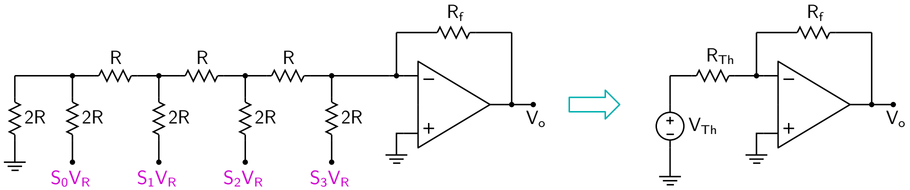
$$= \frac{V_R}{16}\left[S_0\,2^0 + S_1\,2^1 + S_2\,2^2 + S_3\,2^3\right] .$$

* We can use the R-$2R$ ladder network and an op-amp to make up a DAC $\rightarrow$ next slide.

DAC with R-2R ladder

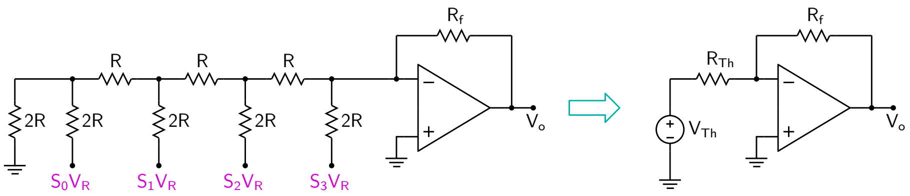


DAC with R-2R ladder



* $V_o = -\dfrac{R_f}{R_{Th}}\, V_{Th} = -\dfrac{R_f}{R_{Th}}\, \dfrac{V_R}{16}\, \left[S_0\, 2^0 + S_1\, 2^1 + S_2\, 2^2 + S_3\, 2^3 \right]\, .$

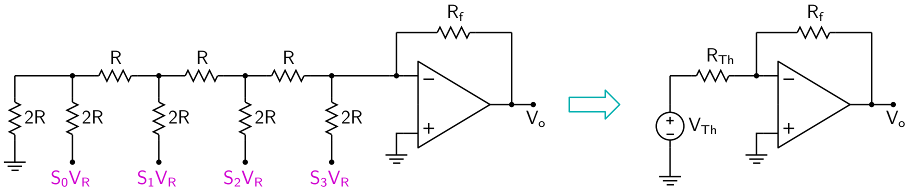
DAC with R-2R ladder



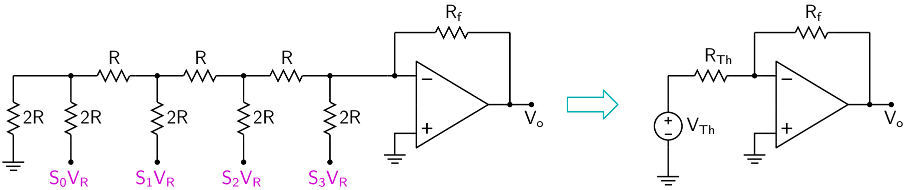
* $V_o = -\dfrac{R_f}{R_{Th}}\,V_{Th} = -\dfrac{R_f}{R_{Th}}\,\dfrac{V_R}{16}\left[S_0\,2^0 + S_1\,2^1 + S_2\,2^2 + S_3\,2^3\right]$.

* For an N-bit DAC, $V_o = -\dfrac{R_f}{R_{Th}}\,V_{Th} = -\dfrac{R_f}{R_{Th}}\,\dfrac{V_R}{2^N}\sum_{0}^{N-1} S_k 2^k$.

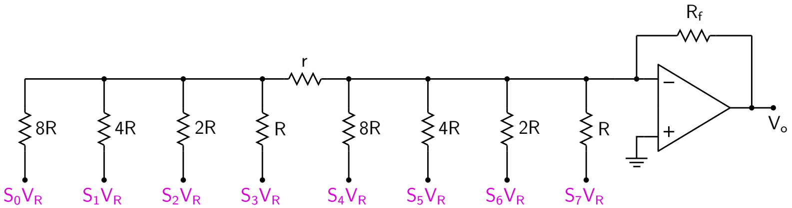
DAC with R-2R ladder



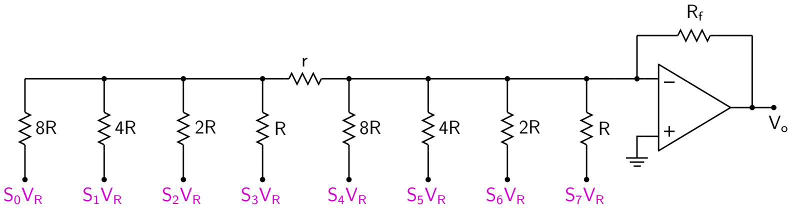
* $V_o = -\dfrac{R_f}{R_{Th}} V_{Th} = -\dfrac{R_f}{R_{Th}} \dfrac{V_R}{16} \left[S_0\, 2^0 + S_1\, 2^1 + S_2\, 2^2 + S_3\, 2^3 \right]$.
* For an N-bit DAC, $V_o = -\dfrac{R_f}{R_{Th}} V_{Th} = -\dfrac{R_f}{R_{Th}} \dfrac{V_R}{2^N} \sum_{0}^{N-1} S_k 2^k$.
* 6- to 20-bit DACs based on the R-2R ladder network are commercially available in monolithic form (single chip).



* $V_o = -\dfrac{R_f}{R_{Th}} V_{Th} = -\dfrac{R_f}{R_{Th}} \dfrac{V_R}{16} \left[S_0\, 2^0 + S_1\, 2^1 + S_2\, 2^2 + S_3\, 2^3 \right]$.
* For an N-bit DAC, $V_o = -\dfrac{R_f}{R_{Th}} V_{Th} = -\dfrac{R_f}{R_{Th}} \dfrac{V_R}{2^N} \sum_{0}^{N-1} S_k 2^k$.
* 6- to 20-bit DACs based on the R-2R ladder network are commercially available in monolithic form (single chip).
* Bipolar, CMOS, or BiCMOS technology is used for these DACs.

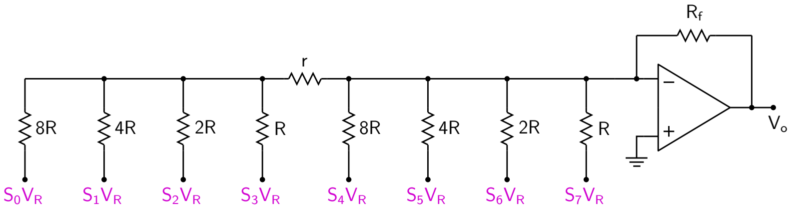


Combination of weighted–resistor and R–2R ladder networks



Combination of weighted–resistor and R–2R ladder networks

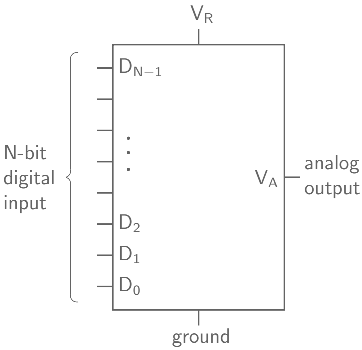
* Find the value of r for the circuit to work as a regular (i.e., binary to analog) DAC.

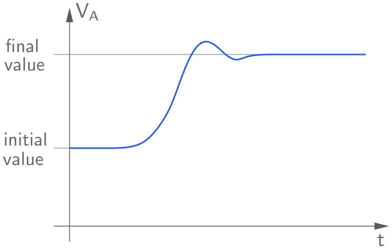


Combination of weighted–resistor and R–2R ladder networks

* Find the value of r for the circuit to work as a regular (i.e., binary to analog) DAC.
* Find the value of r for the circuit to work as a BCD to analog DAC.

DAC: settling time





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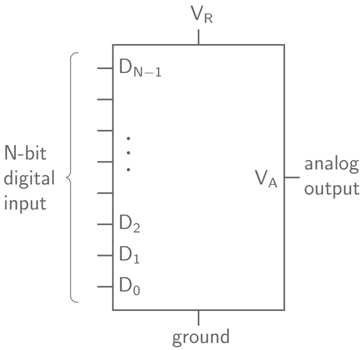
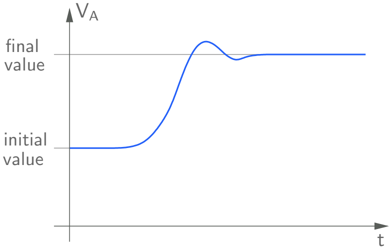
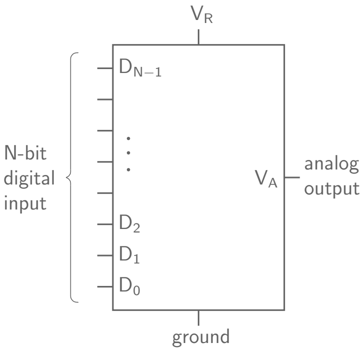
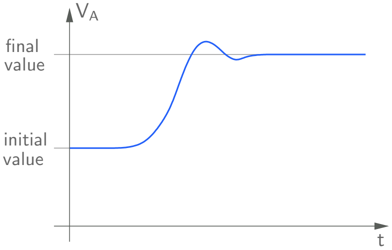




* When there is a change in the input binary number, the output V_A takes a finite time to settle to the new value.

DAC: settling time





* When there is a change in the input binary number, the output V_A takes a finite time to settle to the new value.
* The finite settling time arises because of stray capacitances and switching delays of the semiconductor devices used within the DAC chip.

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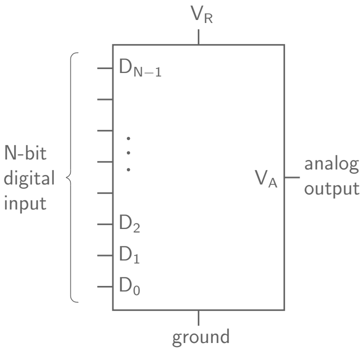
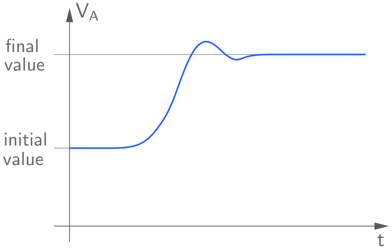
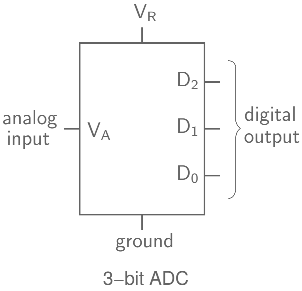
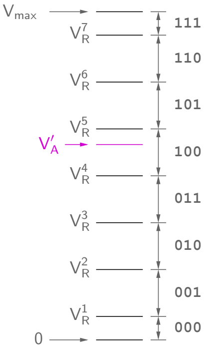


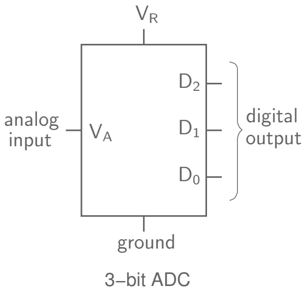


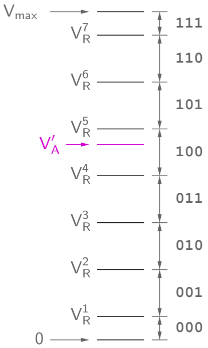
* When there is a change in the input binary number, the output V_A takes a finite time to settle to the new value.
* The finite settling time arises because of stray capacitances and switching delays of the semiconductor devices used within the DAC chip.
* Example: 500 ns to 0.2 % of full scale.

ADC: introduction



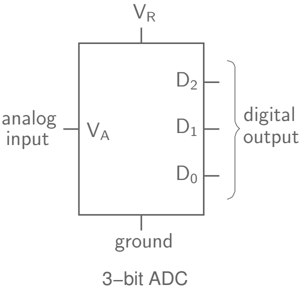


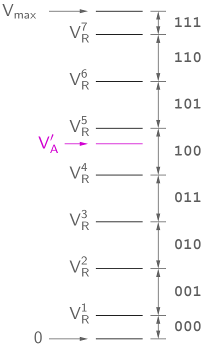




* If the input V_A is in the range $V_R^k < V_A < V_R^{k+1}$, the output is the binary number corresponding to the integer k. For example, for $V_A = V_A'$, the output is 100.

ADC: introduction





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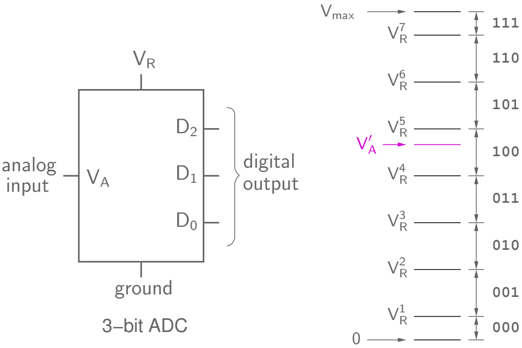

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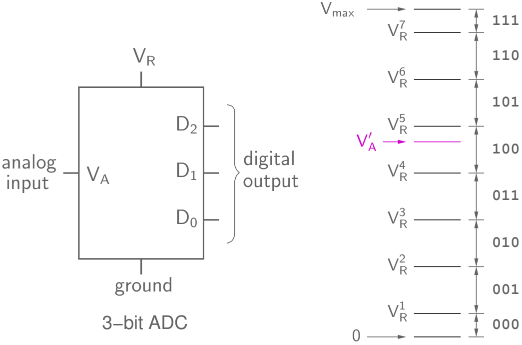
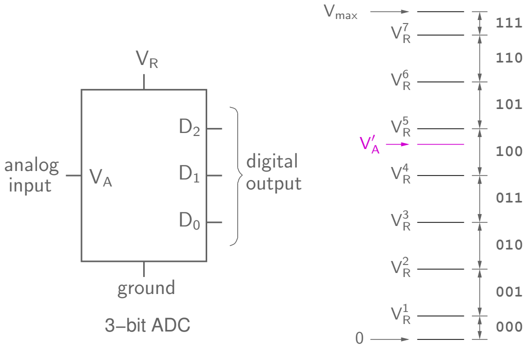
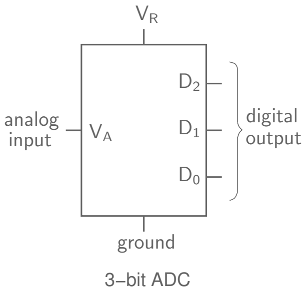
* We may think of each voltage interval (corresponding to 000, 001, etc.) as a "bin." In the above example, the input voltage V_A' falls in the 100 bin; therefore, the output of the ADC would be 100.
* Note that, for an N-bit ADC, there would be 2^N bins.

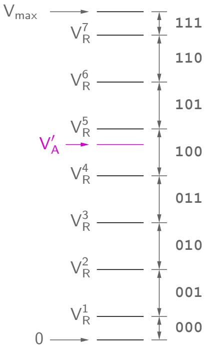
ADC: introduction





* The basic idea behind an ADC is simple:





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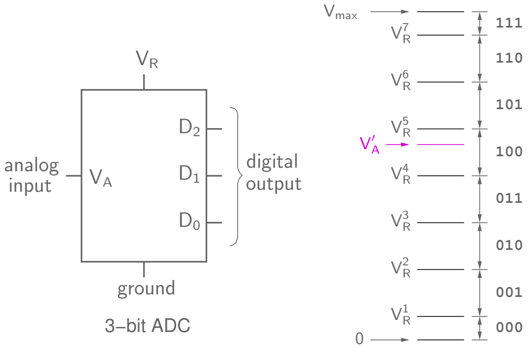
ADC: introduction



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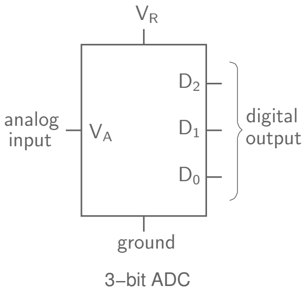

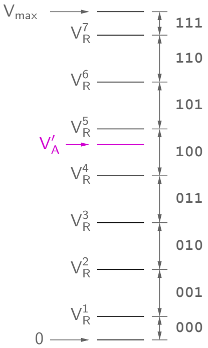

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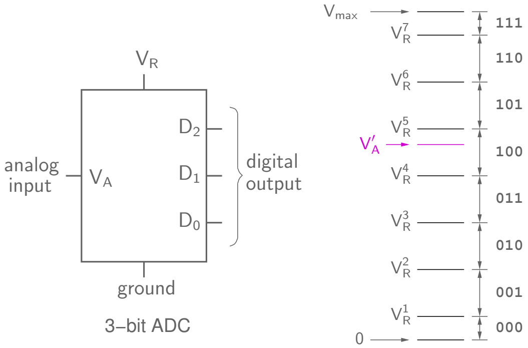

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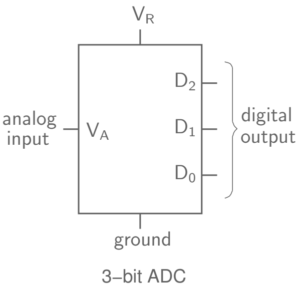
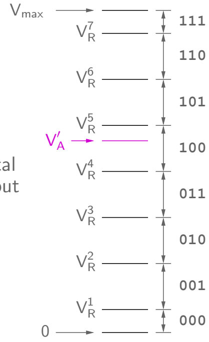
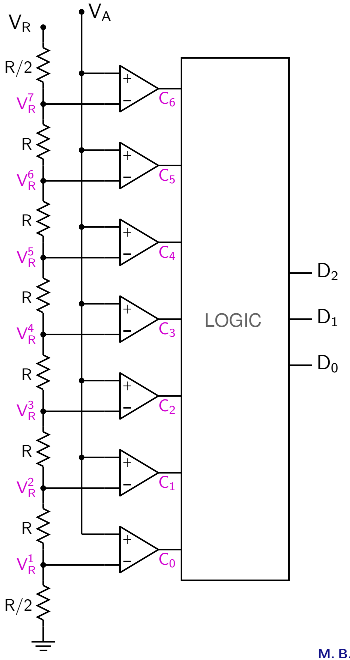
  - If V_A belongs to bin k (i.e., $V_R^k < V_A < V_R^{k+1}$), convert k to the binary format.
* A "parallel" ADC does exactly that → next slide.

3-bit parallel (flash) ADC







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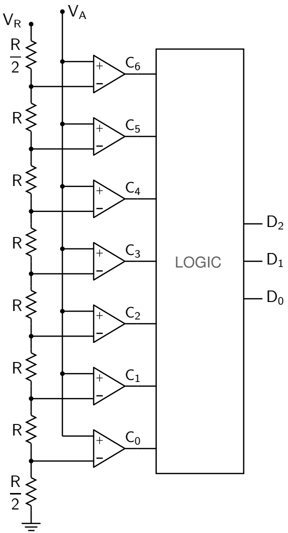

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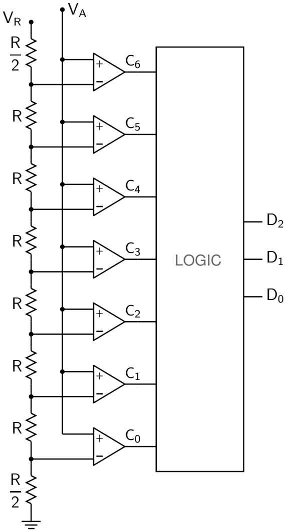

* Practical difficulty: As the input changes, the comparator outputs (C_0, C_1, etc.) may not settle to their new values at the same time. → ADC output will depend on when we sample it.

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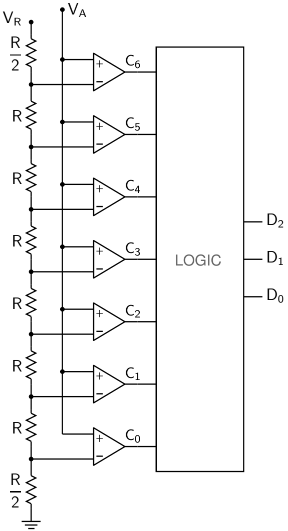

* Practical difficulty: As the input changes, the comparator outputs (C_0, C_1, etc.) may not settle to their new values at the same time. $\rightarrow$ ADC output will depend on when we sample it.
* Add D flip-flops. Allow sufficient time (between the change in V_A and the active clock edge) so that the comparator outputs have already settled to their new values before they get latched in.

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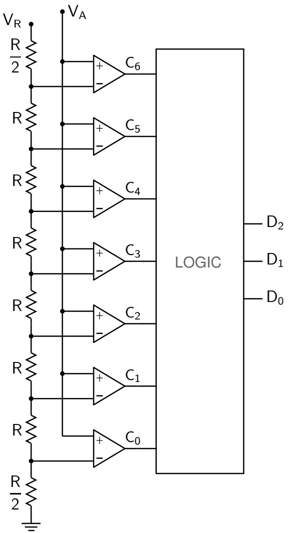

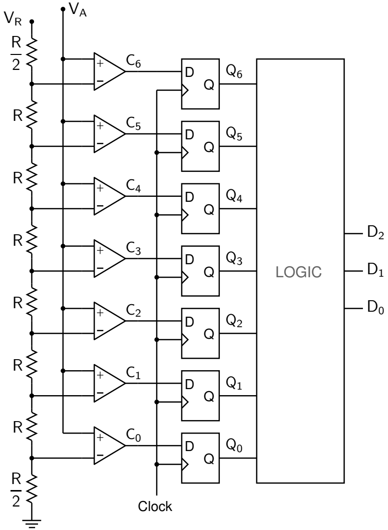

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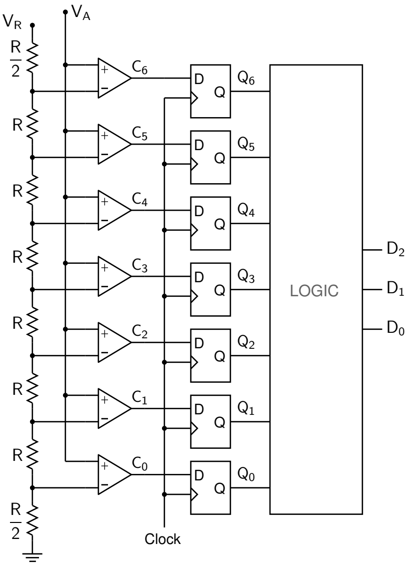
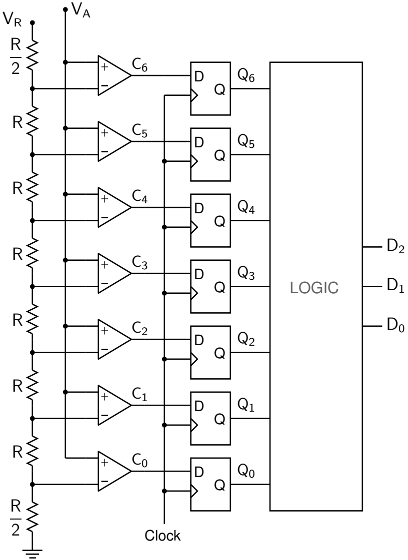
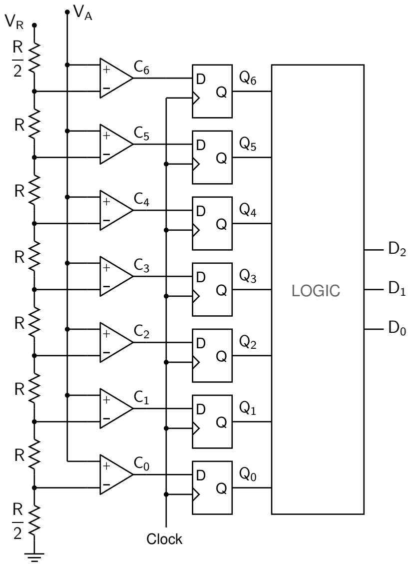


* In the parallel (flash) ADC, the conversion gets done "in parallel," since all comparators operate on the same input voltage.



* In the parallel (flash) ADC, the conversion gets done "in parallel," since all comparators operate on the same input voltage.
* Conversion time is governed only by the comparator response time $\rightarrow$ fast conversion (hence the name "flash" converter).

Parallel (flash) ADC



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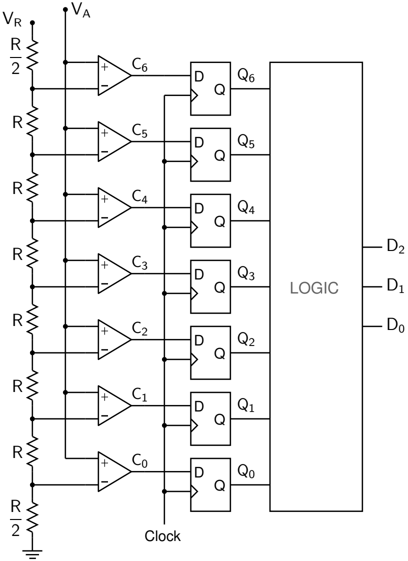

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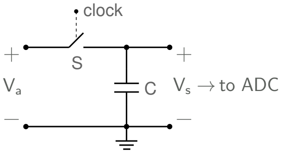
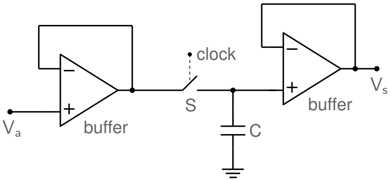
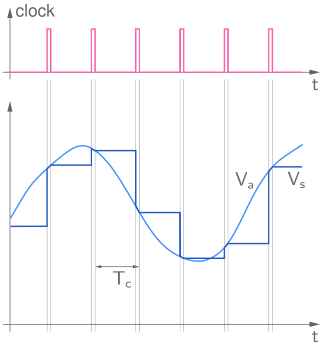
* 2^N comparators are required for N-bit ADC $\rightarrow$ generally limited to 8 bits.

ADC: sampling of input signal







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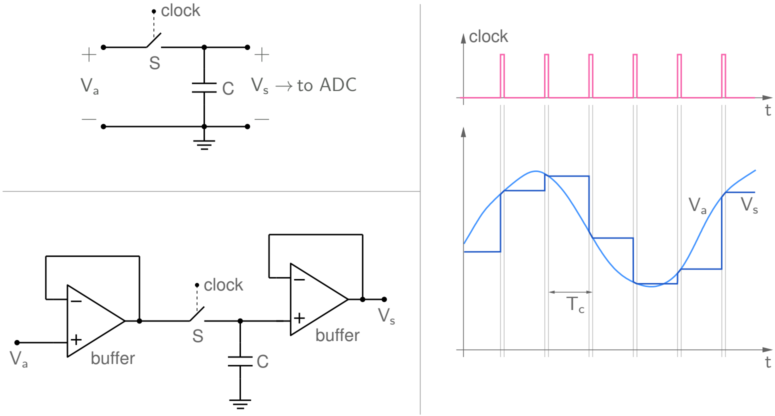

* An ADC typically operates on a "sampled" input signal ($V_s(t)$ in the figure) which is derived from the continuously varying input signal ($V_a(t)$ in the figure) with a "sample-and-hold" (S/H) circuit.

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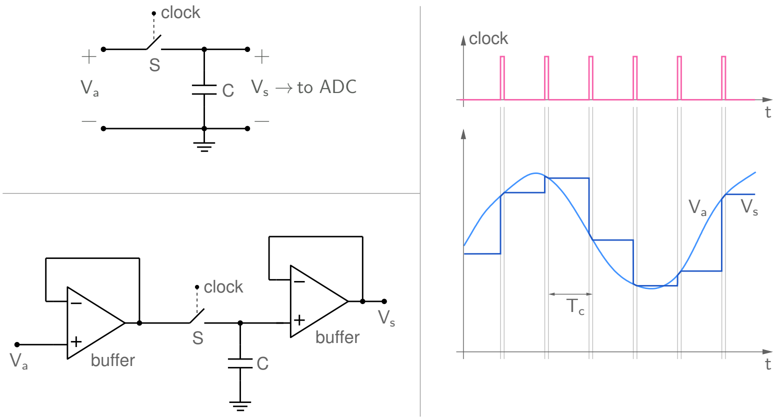

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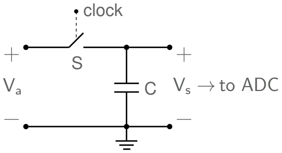

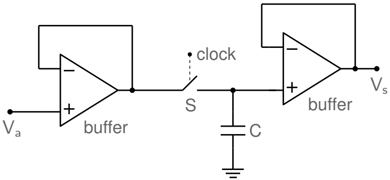

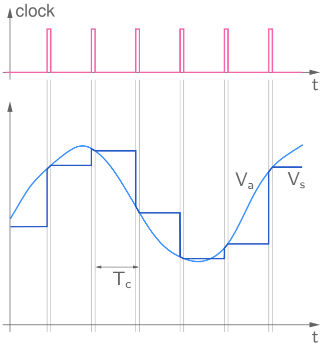

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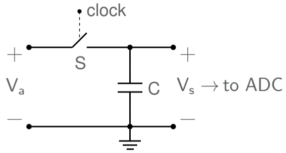

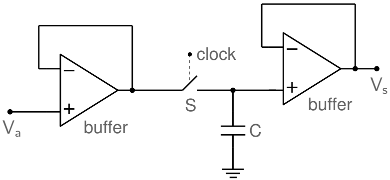

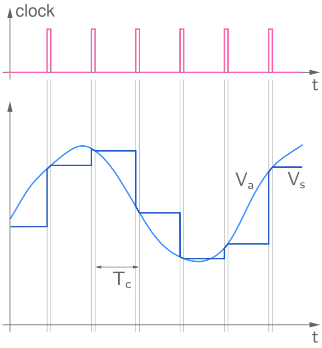

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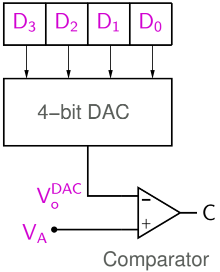
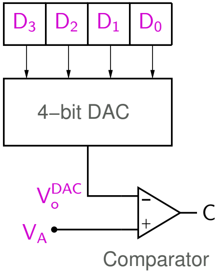
* Op-amp buffers can be used to minimise loading effects.

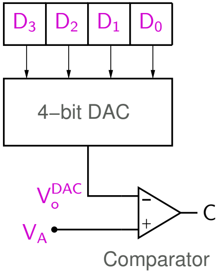
Successive Approximation ADC





* Suppose we have a 4-bit DAC. We can use it to perform A-to-D conversion by successively setting the four bits as follows.

Successive Approximation ADC



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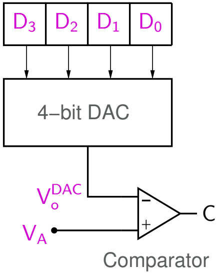

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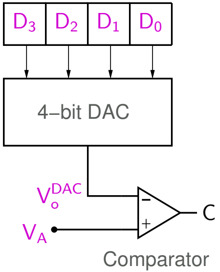

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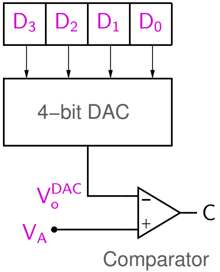
  - Start with $D_3D_2D_1D_0 = 0000$, $\mathtt{I} = 3$.
  - Set $D[\mathtt{I}] = 1$ (keep other bits unchanged).
  - If $V_o^{DAC} > V_A$ (i.e., $C = 0$), set $D[\mathtt{I}] = 0$; else, keep $D[\mathtt{I}] = 1$.

Successive Approximation ADC



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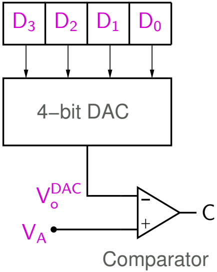
    - Start with $D_3 D_2 D_1 D_0 = 0000$, $\mathrm{I} = 3$.
    - Set $D[\mathrm{I}] = 1$ (keep other bits unchanged).
    - If $V_o^{DAC} > V_A$ (i.e., $C = 0$), set $D[\mathrm{I}] = 0$; else, keep $D[\mathrm{I}] = 1$.
    - $\mathrm{I} \leftarrow \mathrm{I} - 1$; go to step 1.

Successive Approximation ADC



* Suppose we have a 4-bit DAC. We can use it to perform A-to-D conversion by successively setting the four bits as follows.
  - Start with $D_3 D_2 D_1 D_0 = 0000$, $\mathtt{I} = 3$.
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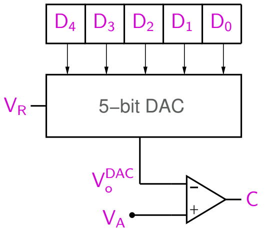
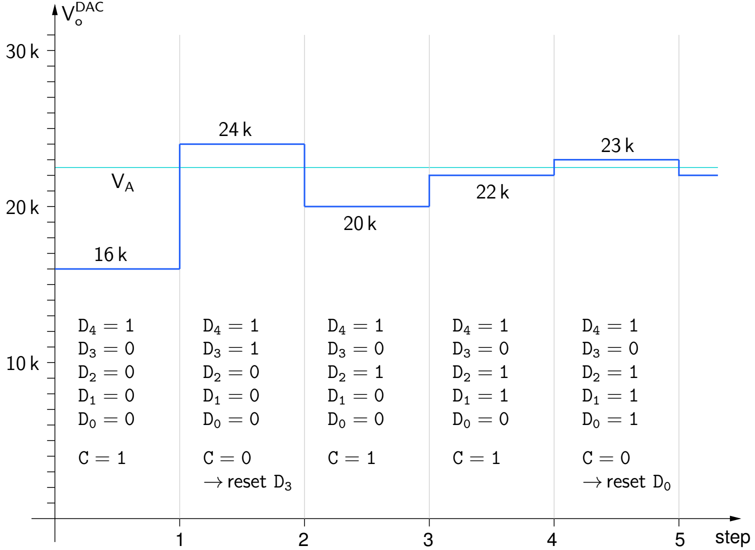
  - $\mathtt{I} \leftarrow \mathtt{I} - 1$; go to step 1.
* At the end of four steps, the digital output is given by $D_3 D_2 D_1 D_0$.
  Example $\rightarrow$ next slide.

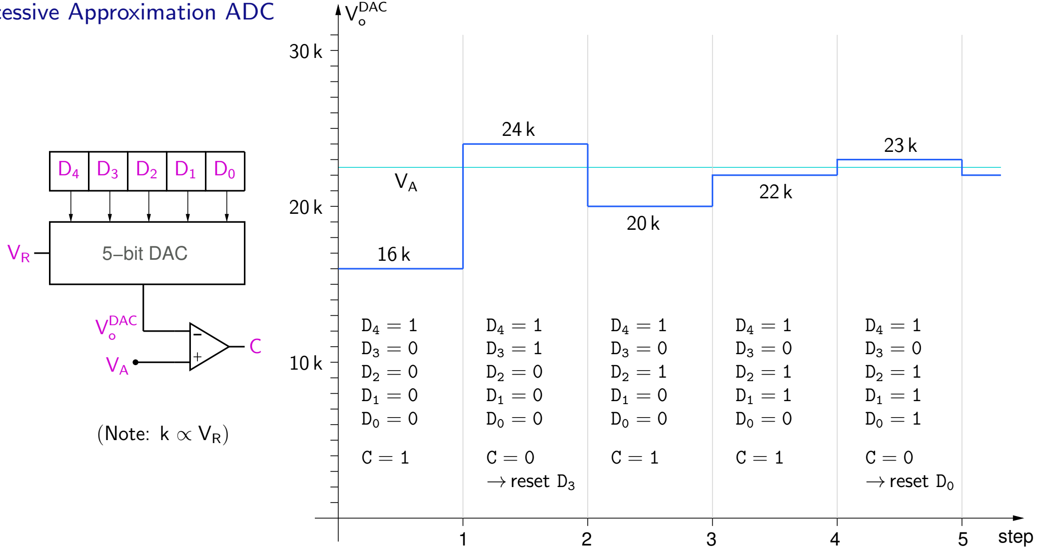
Successive Approximation ADC



(Note: $k \propto V_R$)

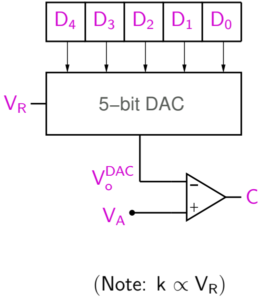


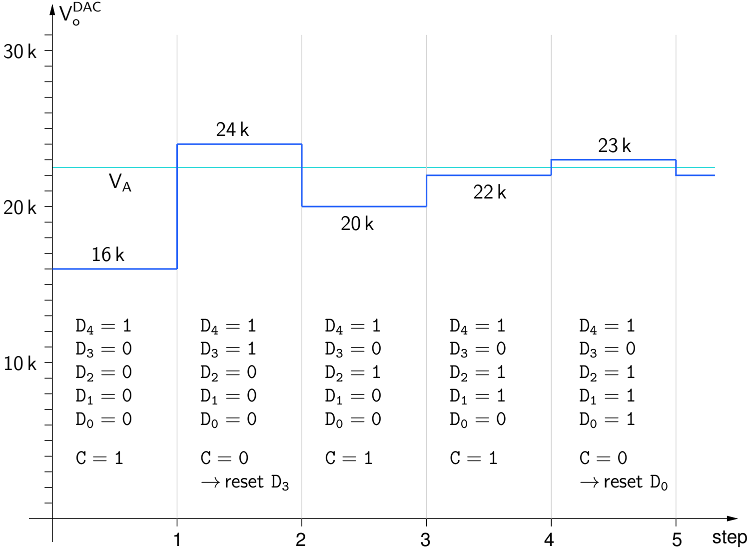
Successive Approximation ADC



* At the end of the 5th step, we know that the input voltage corresponds to 10110.

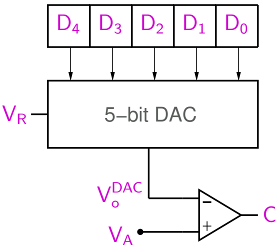
Successive Approximation ADC

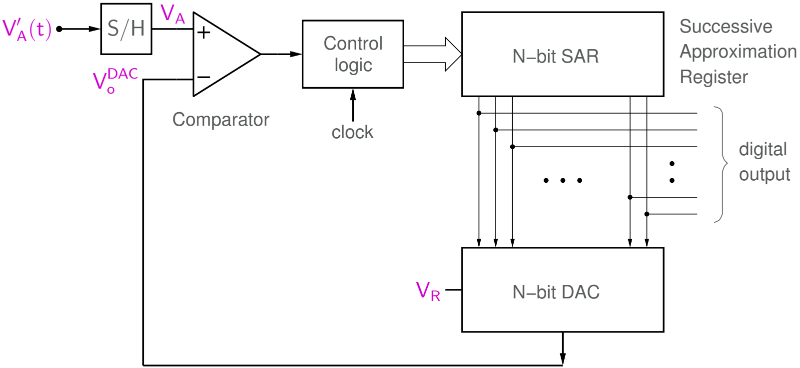




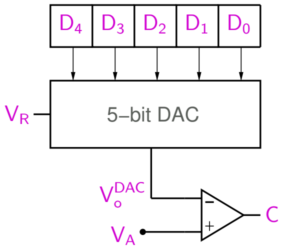
* At the end of the 5th step, we know that the input voltage corresponds to 10110.
* For the digital representation to be accurate up to $\pm\frac{1}{2}$ LSB, ΔV corresponding to $\frac{1}{2}$ LSB is added to V_A (see [Taub]).

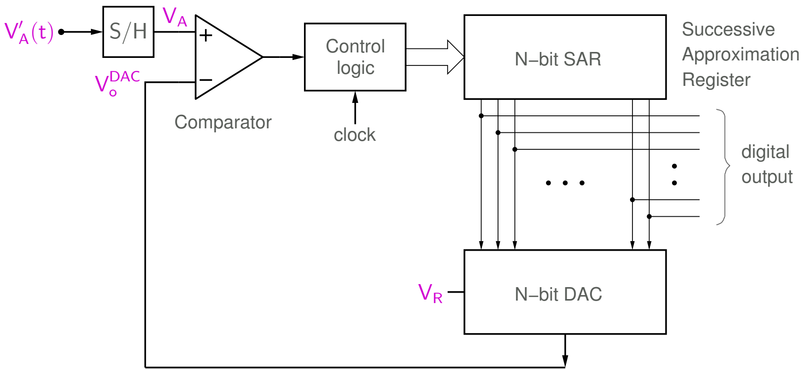
Successive Approximation ADC





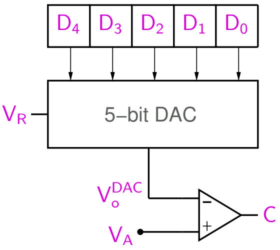
Successive Approximation ADC

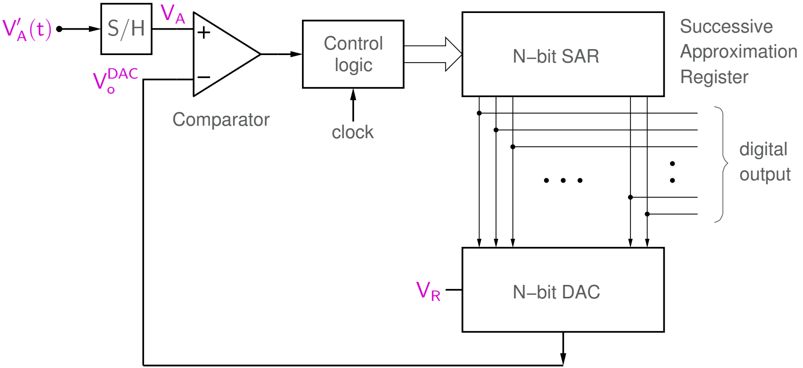




* Each step (setting SAR bits, comparison of V_A and V_o^{DAC}) is performed in one clock cycle $\rightarrow$ conversion time is N cycles, irrespective of the input voltage value V_A.

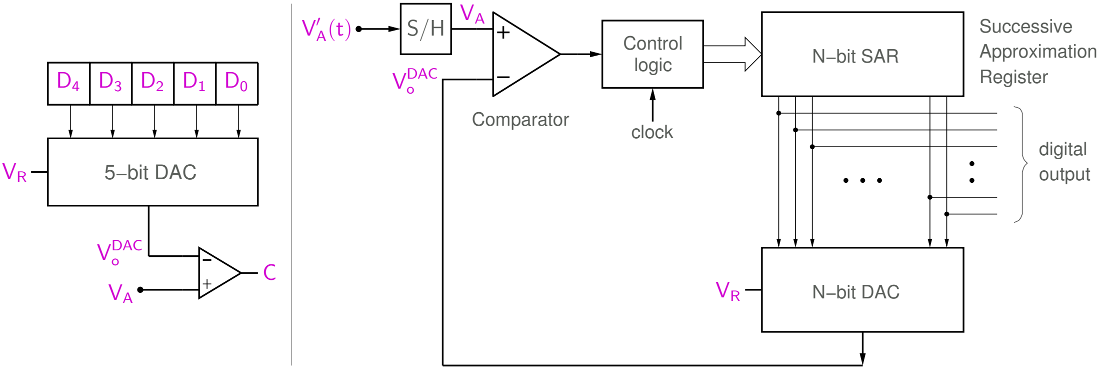
Successive Approximation ADC





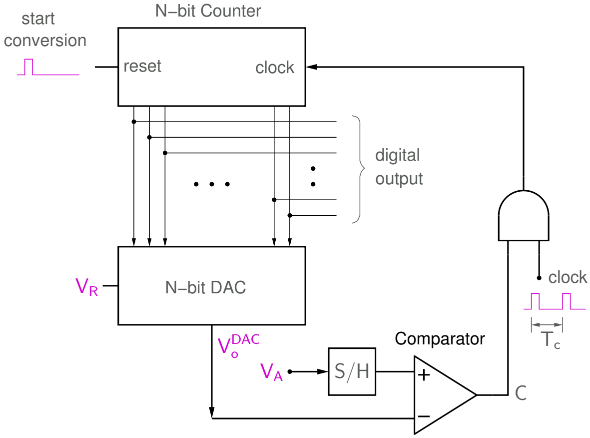
* Each step (setting SAR bits, comparison of V_A and V_o^{DAC}) is performed in one clock cycle $\rightarrow$ conversion time is N cycles, irrespective of the input voltage value V_A.
* S. A. ADCs with built-in or external S/H (sample-and-hold) are available for 8- to 16-bit resolution and conversion times of a few μsec to tens of μsec.

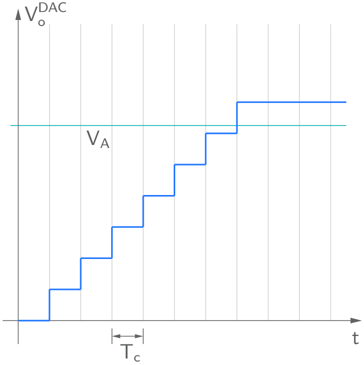
Successive Approximation ADC



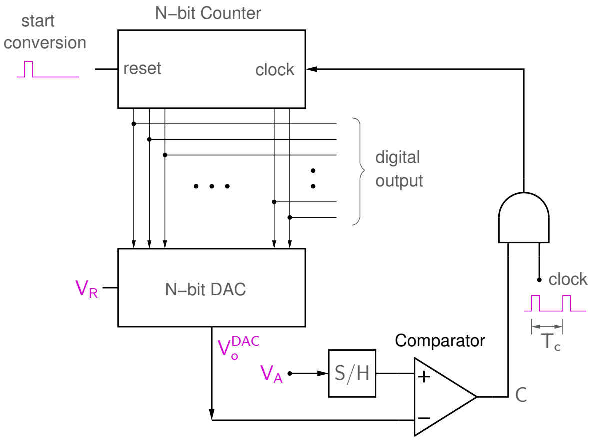
* Each step (setting SAR bits, comparison of V_A and V_o^{DAC}) is performed in one clock cycle $\rightarrow$ conversion time is N cycles, irrespective of the input voltage value V_A.
* S. A. ADCs with built-in or external S/H (sample-and-hold) are available for 8- to 16-bit resolution and conversion times of a few μsec to tens of μsec.
* Useful for medium-speed applications such as speech transmission with PCM.

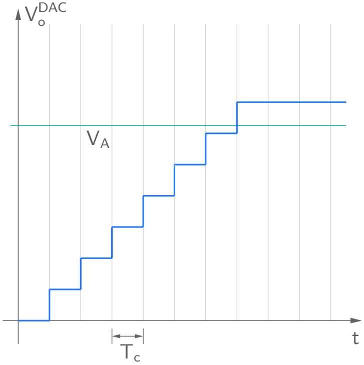
Counting ADC (digital-ramp ADC)





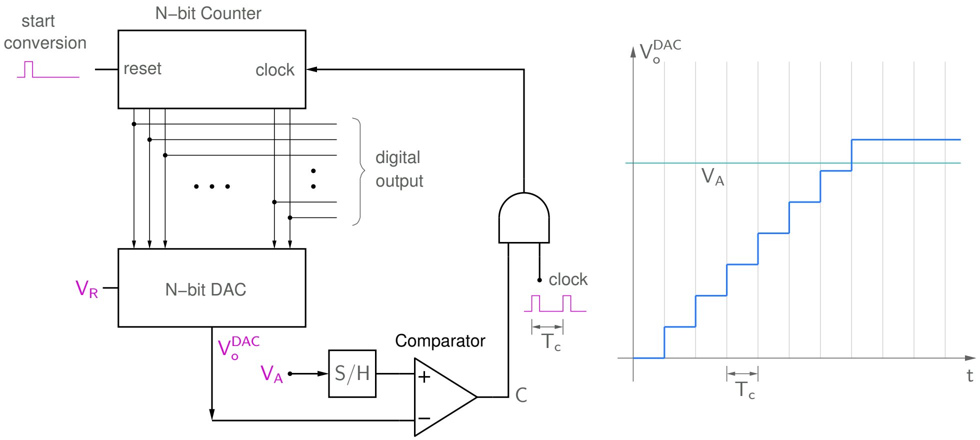
Counting ADC (digital-ramp ADC)





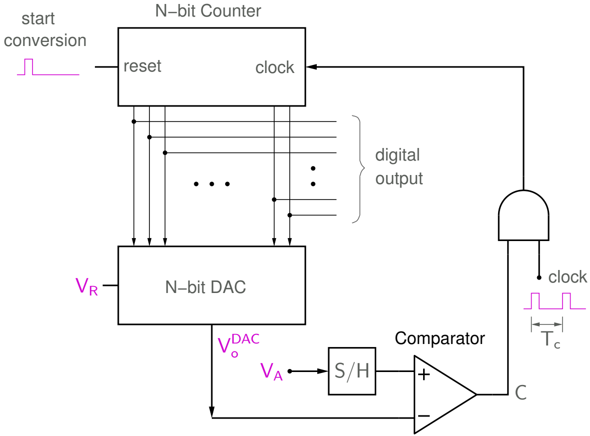
∗ The "start conversion" signal clears the counter; counting begins, and V_o^{DAC} increases with each clock cycle.

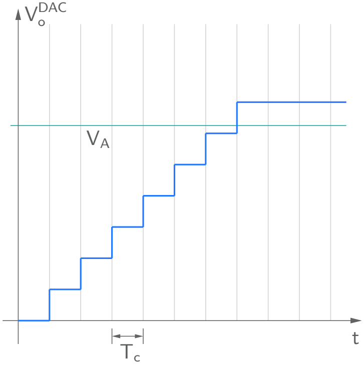
Counting ADC (digital-ramp ADC)



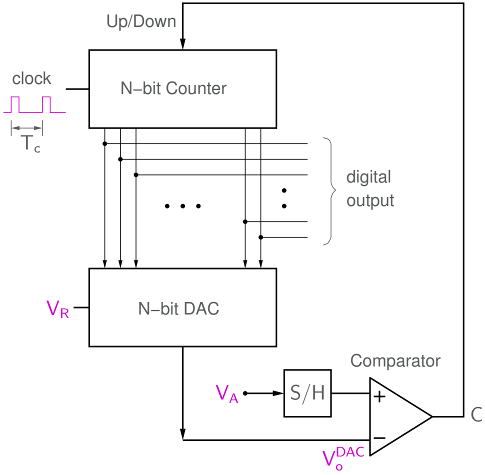
* The "start conversion" signal clears the counter; counting begins, and V_o^{DAC} increases with each clock cycle.
* When V_o^{DAC} exceeds V_A, C becomes 0, and counting stops.

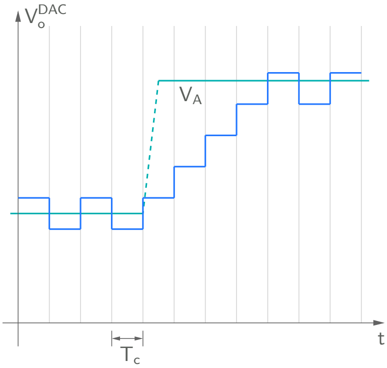
Counting ADC (digital-ramp ADC)

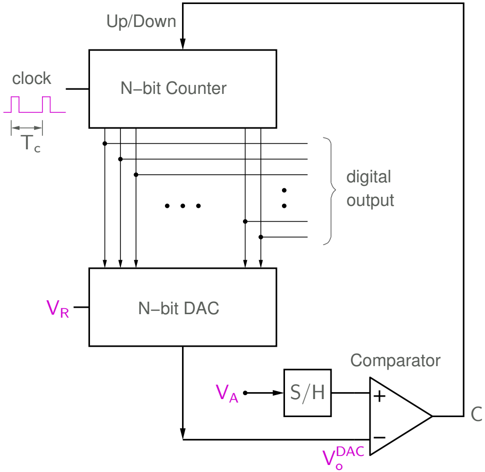


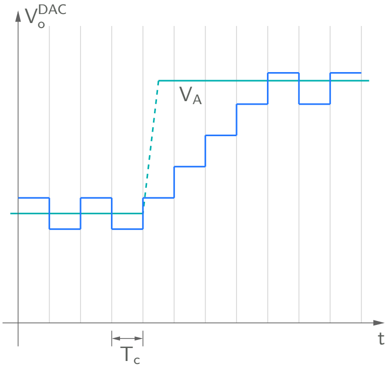


* The "start conversion" signal clears the counter; counting begins, and V_o^{DAC} increases with each clock cycle.
* When V_o^{DAC} exceeds V_A, C becomes 0, and counting stops.
* Simple scheme, but (a) conversion time depends on V_A, (b) slow (takes $(2^N - 1)$ clock cycles in the worst case) $\rightarrow$ tracking ADC

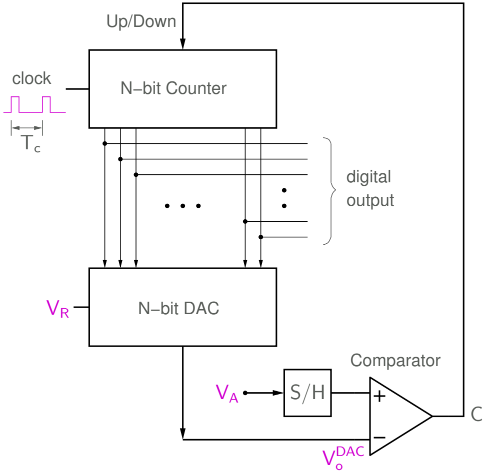

Up/Down
clock
T_c
N–bit Counter
digital output
V_R
N–bit DAC
Comparator
V_A
S/H
+
−
V_o^{DAC}
C

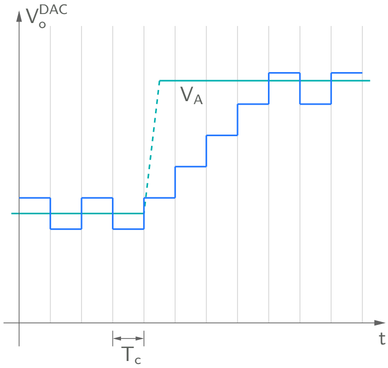

V_o^{DAC}
V_A
T_c
t





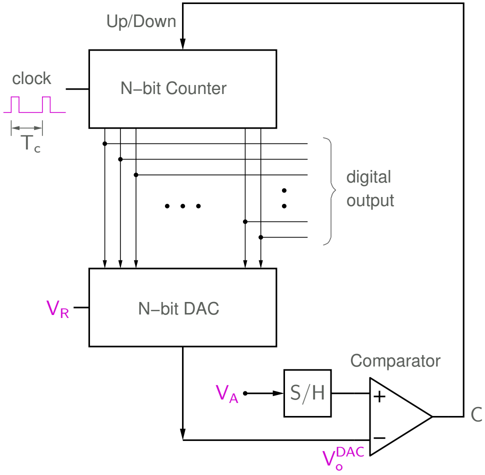
* The counter counts up if $V_o^{DAC} < V_A$; else, it counts down.

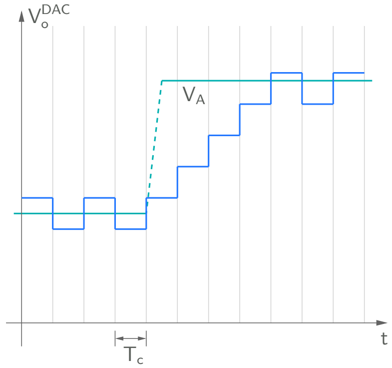




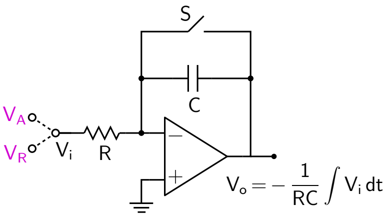
* The counter counts up if $V_o^{DAC} < V_A$; else, it counts down.
* If V_A changes, the counter does not need to start from $000 \cdots 0$, so the conversion time is less than that required by a counting ADC.

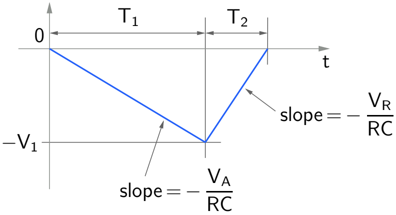
Tracking ADC

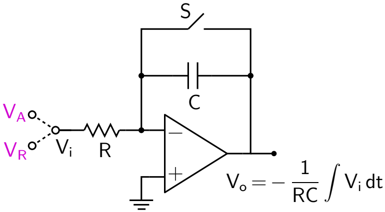


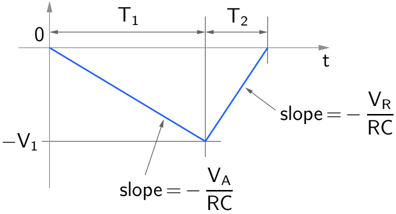


* The counter counts up if $V_o^{DAC} < V_A$; else, it counts down.
* If V_A changes, the counter does not need to start from $000 \cdots 0$, so the conversion time is less than that required by a counting ADC.
* used in low-cost, low-speed applications, e.g., measuring output from a temperature sensor or a strain gauge

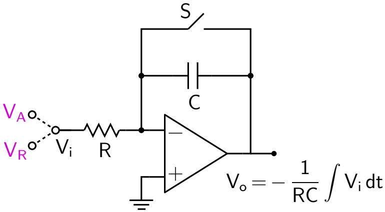

S
C
V_A
V_R
V_i
R
$V_o = -\frac{1}{RC}\int V_i\,dt$

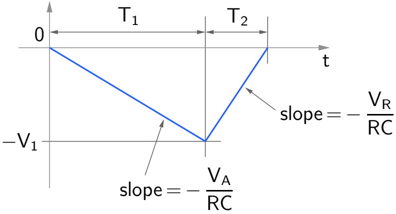

T_1
T_2
0
t
$-V_1$
$\text{slope} = -\frac{V_R}{RC}$
$\text{slope} = -\frac{V_A}{RC}$





* $t = 0$: reset integrator output V_o to 0 V by closing S momentarily.





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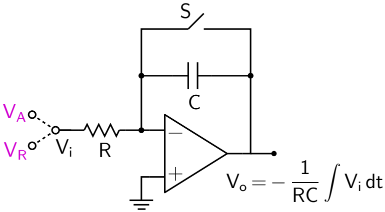
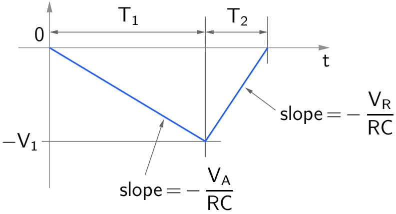
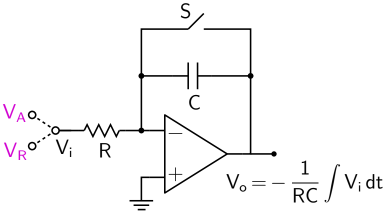
* Integrate V_A (voltage to be converted to digital format, assumed to be positive) for a fixed interval T_1.

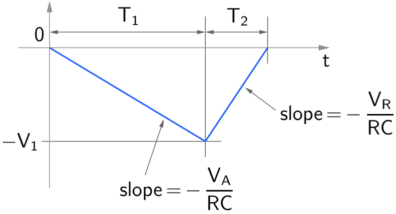




* $t = 0$: reset integrator output V_o to 0 V by closing S momentarily.
* Integrate V_A (voltage to be converted to digital format, assumed to be positive) for a fixed interval T_1.
* At $t = T_1$, integrator output reaches $-V_1 = -\,V_A\,\dfrac{T_1}{RC}$.

Dual-slope ADC





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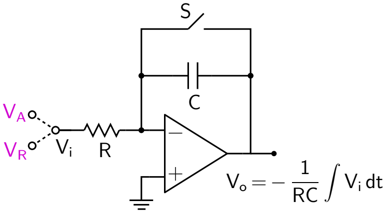
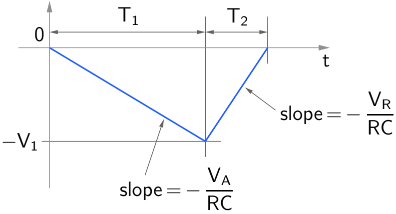
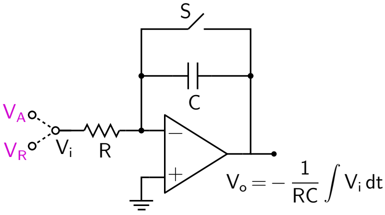
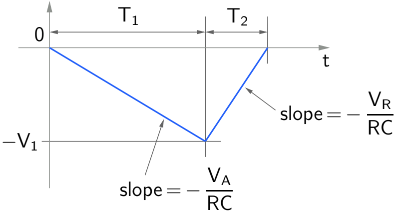
- At $t = T_1$, integrator output reaches $-V_1 = -V_A\,\dfrac{T_1}{RC}$.
- Now apply a reference voltage V_R (assumed to be negative, with $|V_R| > V_A$), and integrate until V_o reaches 0 V.





* $t = 0$: reset integrator output V_o to 0 V by closing S momentarily.
* Integrate V_A (voltage to be converted to digital format, assumed to be positive) for a fixed interval T_1.
* At $t = T_1$, integrator output reaches $-V_1 = -\,V_A\,\dfrac{T_1}{RC}$.
* Now apply a reference voltage V_R (assumed to be negative, with $|V_R| > V_A$), and integrate until V_o reaches 0 V.
* Since $V_1 = V_A\,\dfrac{T_1}{RC} = |V_R|\,\dfrac{T_2}{RC}$, we have $T_2 = T_1\,\dfrac{V_A}{|V_R|} \rightarrow T_2$ gives a measure of V_A.





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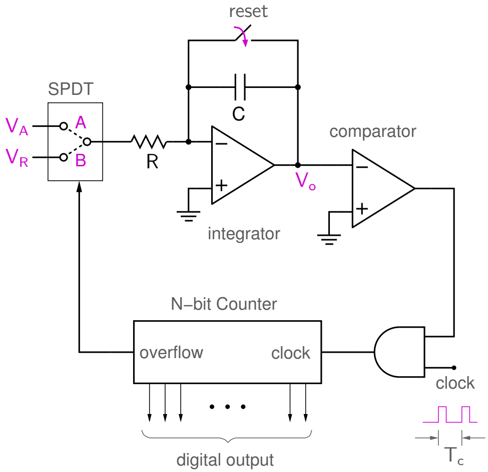
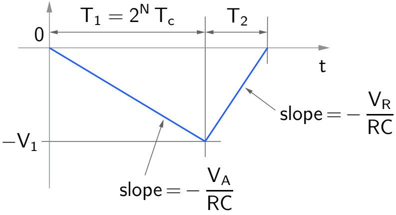
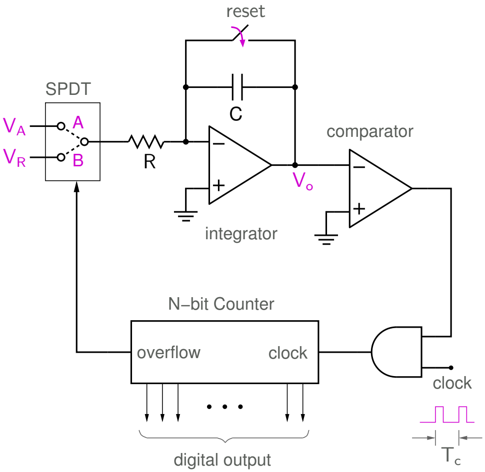
* At $t = T_1$, integrator output reaches $-V_1 = -V_A \dfrac{T_1}{RC}$.
* Now apply a reference voltage V_R (assumed to be negative, with $|V_R| > V_A$), and integrate until V_o reaches 0 V.
* Since $V_1 = V_A \dfrac{T_1}{RC} = |V_R| \dfrac{T_2}{RC}$, we have $T_2 = T_1 \dfrac{V_A}{|V_R|} \rightarrow T_2$ gives a measure of V_A.
* In the dual-slope ADC, a counter output – which is proportional to T_2 – provides the desired digital output.

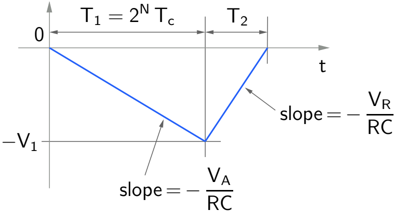
Dual-slope ADC



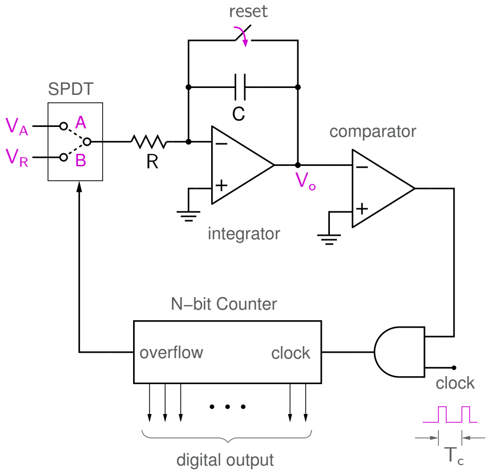


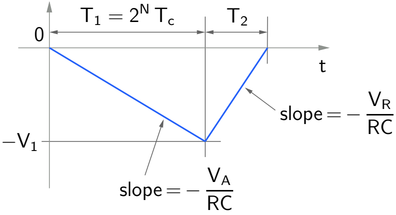
Dual-slope ADC





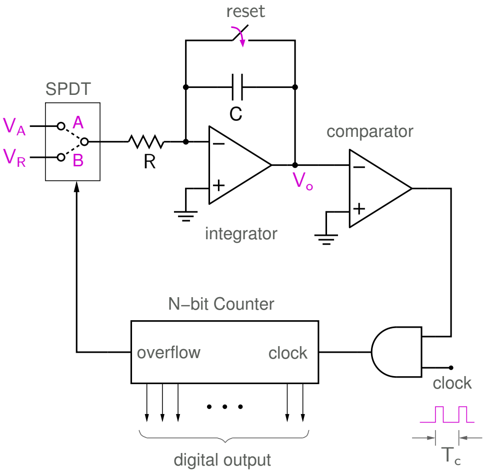
* Start: counter reset to $000 \cdots 0$, SPDT in position A.

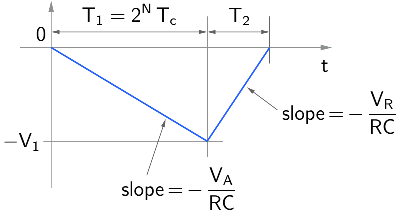




* Start: counter reset to $000\cdots0$, SPDT in position A.
* Counter counts up to 2^N at which point the overflow flag becomes 1, and SPDT switches to position B $\rightarrow$ $T_1 = 2^N\, T_c$ where T_c is the clock period.

Dual-slope ADC





- ∗ Start: counter reset to $000 \cdots 0$, SPDT in position A.
- ∗ Counter counts up to 2^N at which point the overflow flag becomes 1, and SPDT switches to position B $\rightarrow$ $T_1 = 2^N\, T_c$ where T_c is the clock period.
- ∗ The counter starts counting again from $000 \cdots 0$, and stops counting when V_o crosses 0 V. The counter output gives T_2 in binary format.

References

* K. Gopalan, *Introduction to Digital Microelectronic Circuits*, Tata McGraw-Hill, New Delhi, 1978.
* H. Taub and D. Schilling, *Digital Integrated Electronics*, McGraw-Hill, 1977.