Semiconductor Manufacturing

ISSUES

CDEEP
IIT Bombay

Semiconductor Manufacturing is constrained by Requirement of Very Very Clean enviroment during processes. The place where such 'clean' or rather 'Super Clean' enviroment is created is called "CLEAN-ROOM".

All IC manufacturing companies have Three Step approach to control of Contaminants.

1. CLEAN-ROOM [OF Desired "Class"]
2. Wafer Cleaning
3. Gettering

Contaminants may be classified as

1. Particles 2 Surface contaminants

3 Molecular contaminants

1 Particle contamination

(a) Major source are the people working in IC Labs.

(a;) Skin prespiration (a_{ii}) Hair (a_{iii}) Clothing Lints

(b) Bare wood, cardboard products; Including Paper could be Source of Particles

(c) Any machine which produces 'Sawing' or Sanding or Drilling.

2. Surface Contaminants

(a) finger's tips :- Oil and Grease

(b) Oil on body, Hair

(c) Face-Cream, Wax

(d) Polish

(e) Face powder

3. Molecular Contaminants

(a) Out Gassing (b) Oil vapours (c) Paints, Glues & Epoxies

(d) Aromatics (e) Alcohol

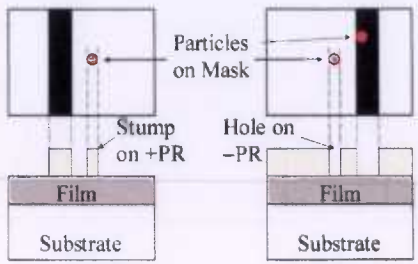
4. Inorganic & Organic Contamination due to equipments and Reagents in Lab.

(a) Heavy Metals – Stainless Steel Pipes, Furnace front ends, other metallic impurities from Reagents

(b) From Water, Human prespiration and air, one gets Alkali Ions who occupy Silicon Surface. Na^+ and K^+ are likely alkali ions in the lab.

[A] Effect of Contaminants

Effect of Particles on Masks



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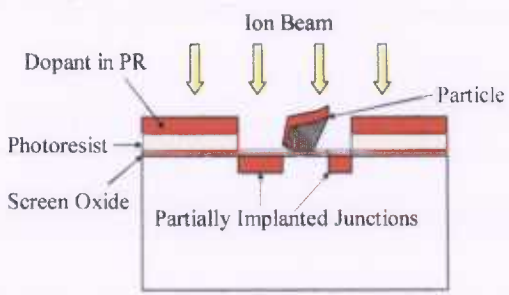
Effect of Particle Contamination



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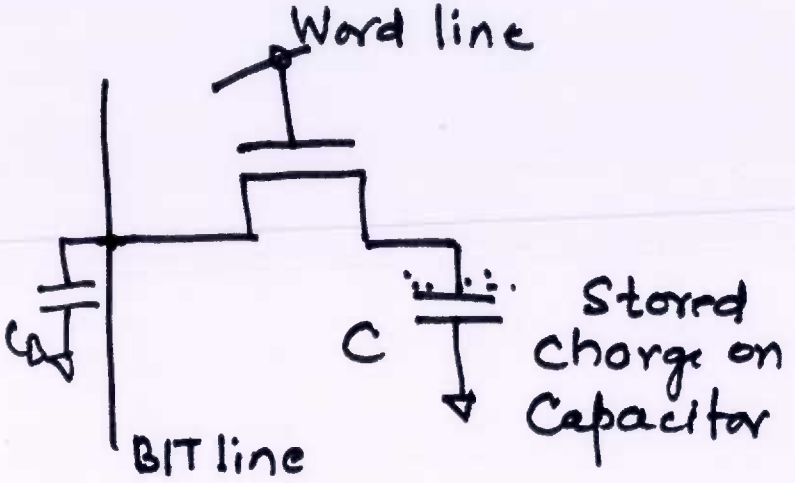
[B] DRAM performance under contaminant environment



DRAM performance :— Refresh time

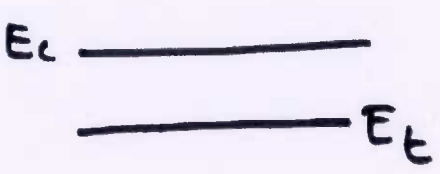
Access time

During Refresh cycle, the generation of ~~elec~~ electrons are needed in the MOS capacitor

For larger time elapse between Refresh Cycles, we need Generation time τ_G be High.

Further loss of DRAM charge is essentially due to Leakage currents. Leakage occures due to Recombination

The SRH mechanism is dominated due to Presence of Traps in Silicon. We know



$$\tau_R = \tau_G = \frac{1}{\sigma \upsilon_{th} \cdot N_t}$$

where N_t is Trap Density

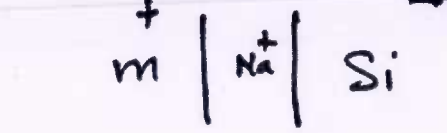
for $\tau_R = \tau_G \geq 100\ \mu s \sim 1$ (or even higher) msec

Min $\tau_R = \tau_G$ as per SIA standards should be $\geq 25\ \mu sec$

For $\upsilon_{th} = 10^7$ cm/sec in Silicon, with Capture Cross section σ of the order of 10^{-15}, the Trap density N_t be $\simeq 10^{12}$/cc. (0.02 ppb). Typical traps availability are due to Na^+, K^+, Au and Fe as well as Cu. First two Na^+ & K^+ are mobile ions on the Surface

[C] Alkali ions (Mobile Ions) can get incorporated in Gate-Oxide of MOS structure. This may give variable V_T

$$V_{T_{n,p}} = \pm\phi_{ms} \pm 2\phi_F - \frac{Q_B + Q_{ox} + Q_m + Q'_{it}}{C_{ox}}$$



Q_M is Mobile Ion (like Na^+) density in col./cm^2

Clearly if Q_M varies due to mobile ion movement, then V_T also varies proportionately.

PBTI and NBTI are known worries in MOS Flash RONs.

Clean Room Concept

1. Site Infrastructure, facilities & Building
2. Power Supply needs and distribution
3. Electrical and Communication systems
4. Main Clean-Room area
5. Surrounding room areas
6. Central facilities
7. Process Utilities
8. Environment and Safety.

Space Allocation in Clean area

1. Lithography : 25 %.
2. Diffusion & LPCVD : 20 %.
3. Ion Implantation : 10 %.
4. Thin Film Deposition : 20 %.
5. Dry Etching : 15 %.
6. Wet-Cleaning areas : 10 %.