Quiz Cum Test - II

30th October 2014

Time: 8.45 PM to 10.00 PM

Venue: GG001 and GG002

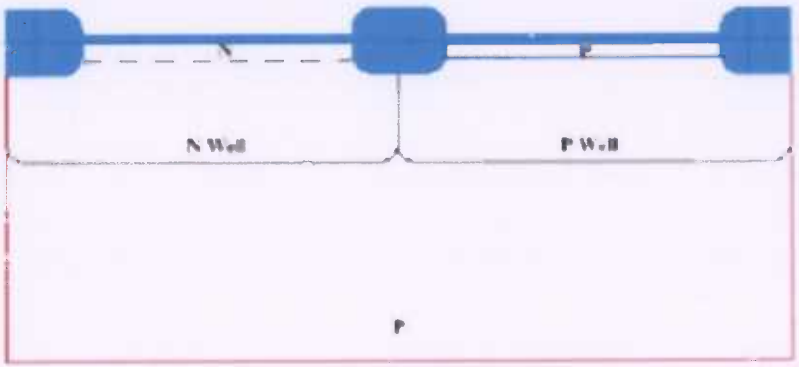
Course:. "After Mid. sem till 29th October

"No" SHEET · during Exam

Polysilicon Gate Realization

CDEEP
IIT Bombay

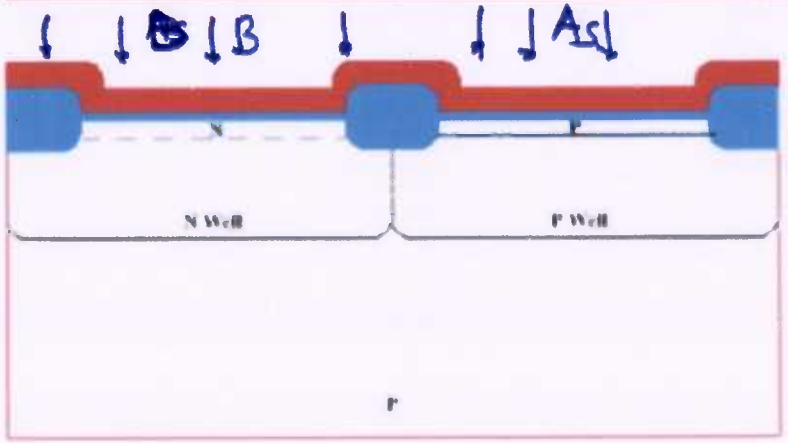
Gate Stack Formation



• Etch back thin oxide and **grow clean gate oxide** ~ 5 nm, which can be grown at 800°C in ~ 1 hr.

Nitrided oxides are typical today, and alternative high-K dielectrics are also being considered for sub 90 nm, Node

Dry Oxidation



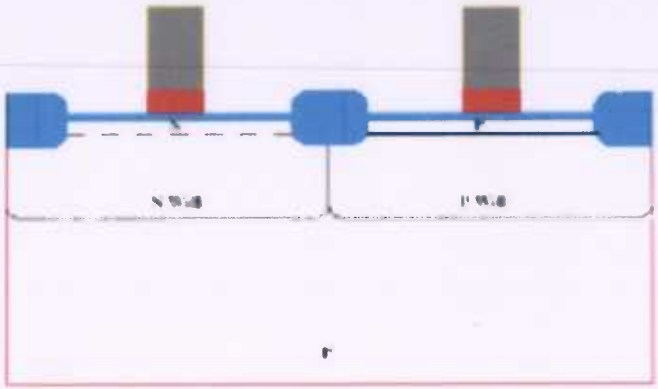
• LPCVD **polysilicon gate deposition** (~0.1 microns). Either masked or unmasked polysilicon doping implant is then performed (target dose such that final average poly doping is > 10^{20} cm^{-3}).

$R_s \simeq$ 10-20 ohm/□

Doping of Poly.
1 In Situ during Poly deposition
2 Solid State Diff.
3. Implant

Gate Delineation

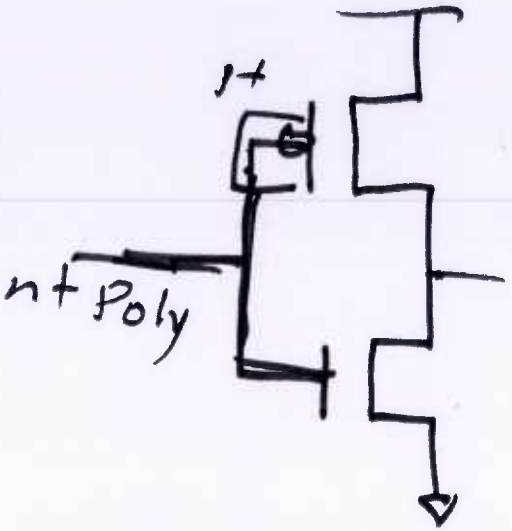
CDEEP
IIT Bombay

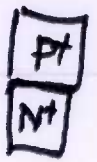


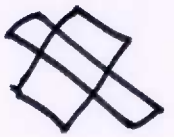
• **Gate etch**: Mask #6 is used to protect the MOS gates. The polysilicon is plasma etched using an anisotropic etch which stops on the underlying oxide.

Process option: **gate re-oxidation** (to improve reliability in very thin gate oxide devices). Must be done carefully to avoid formation of non-uniform gate oxide thickness:

K. Rim, Ph.D. thesis, Stanford Univ.

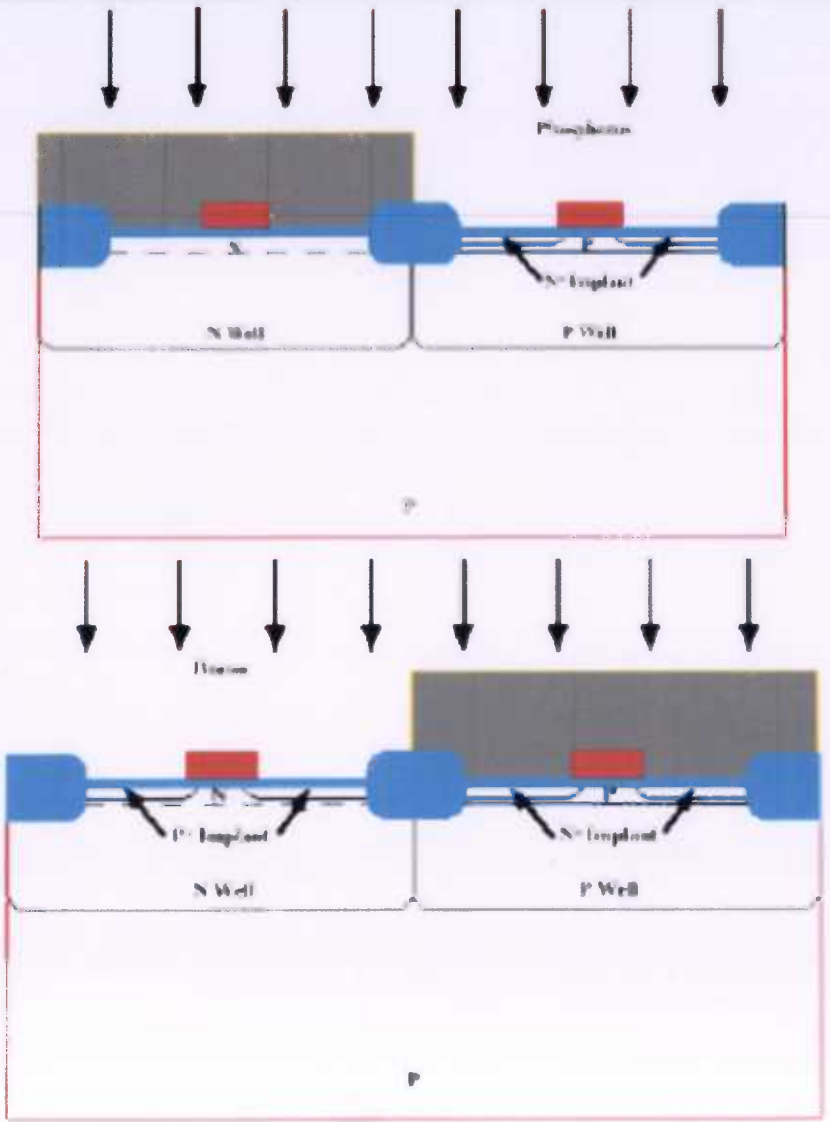






RAG ⇒ Trans.

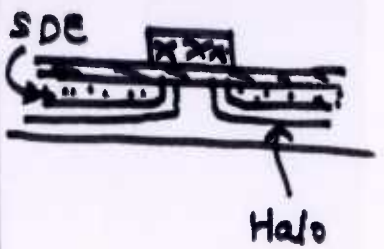
S/D Extensions for SCE reduction



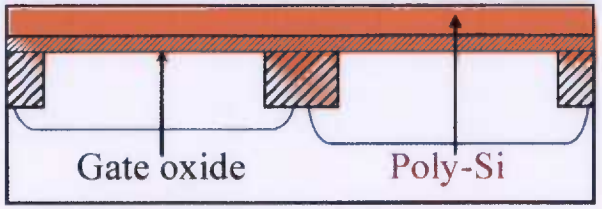
- **NMOS S/D Extension formation:** Original concept was Lightly Doped Drain (LDD) to help deal with hot electron effects. Today, the S/D extension serves to mitigate short channel effects. Mask #7 protects the PMOS devices. An As+ implant forms the LDD regions in the NMOS devices.

- **PMOS S/D Extension formation:** Mask #8 protects the PMOS devices. A B^+ implant forms the LDD or extension regions.

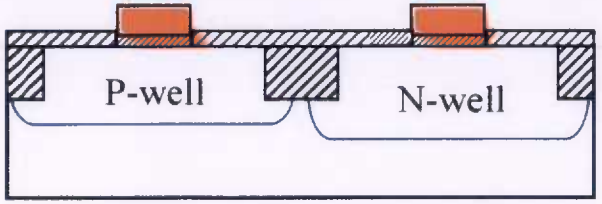
CDEEP
IIT Bombay



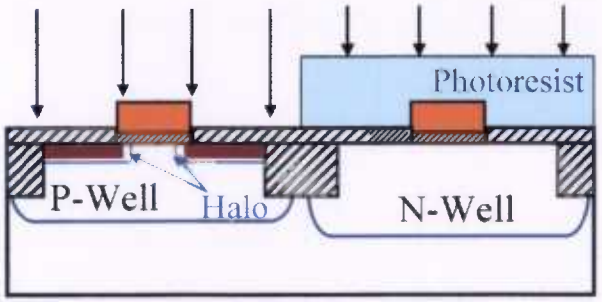
CMOS Fabrication



4 Gate formation:
- Clean silicon surface
- grow gate oxide
- deposit poly-Si gate electrode.

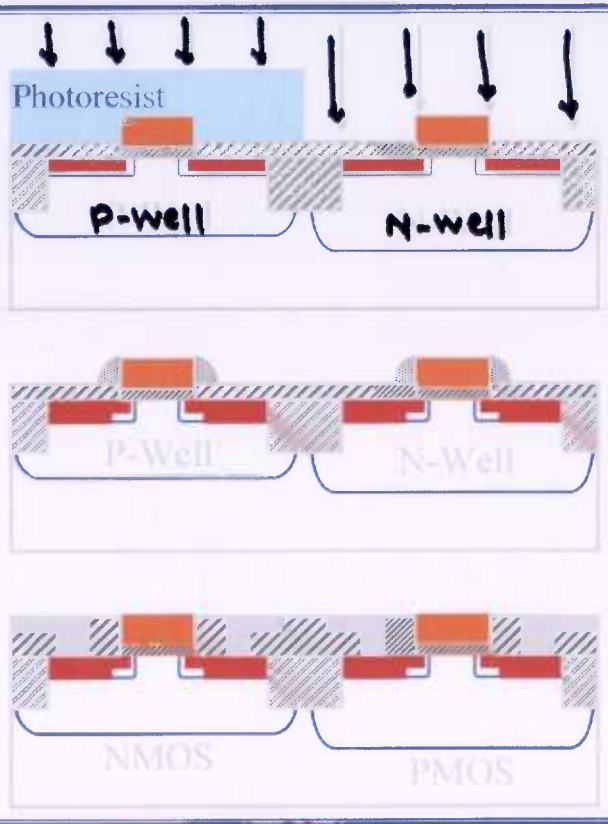


5 Mask #4: Gate definition
- etch poly-Si
- etch oxide
- grow masking oxide.

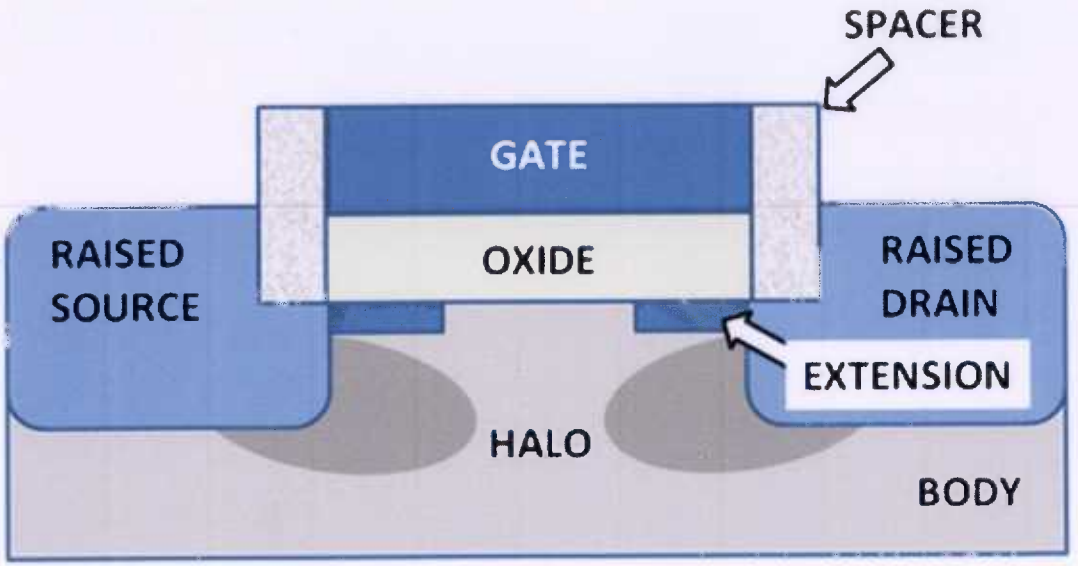


6 Mask #5: N+ source / drain extension (SDE) and p-halo:
- As SDE implant
- B/BF2 halo implant
- clean.

Halo

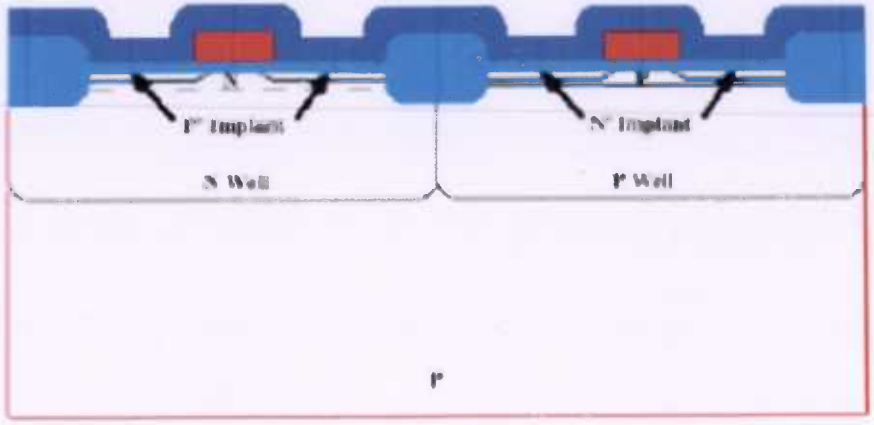


p^+ implant for S&D Extension
n - halo implant


SPACER
GATE
OXIDE
RAISED
SOURCE
RAISED
DRAIN
EXTENSION
HALO
BODY

Sidewall Spacer creation

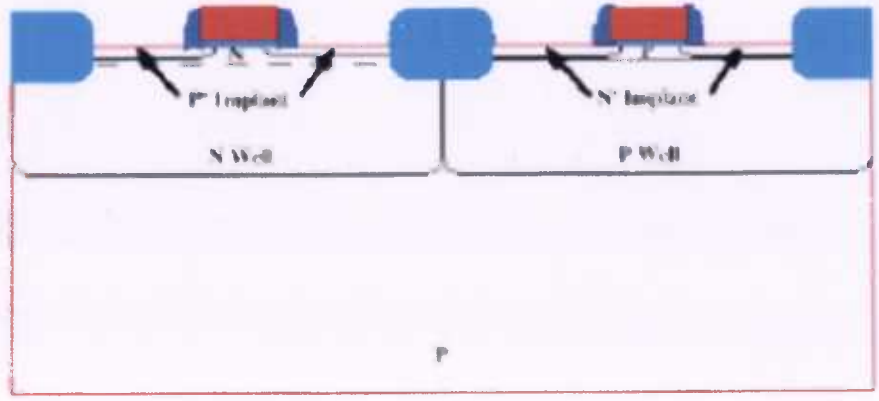
CDEEP
IIT Bombay



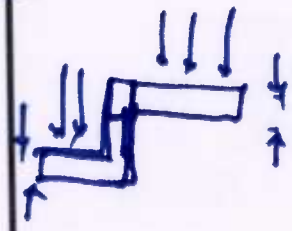
- **Sidewall spacer formation (oxide):**
A conformal layer of SiO_2 is deposited (typically ~ 0.1 to 0.25 microns thick) LPCVD Process.

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

$$SiH_2Cl_2 + N_2O \rightarrow SiO_2 + 2N_2 + 2HCl.$$

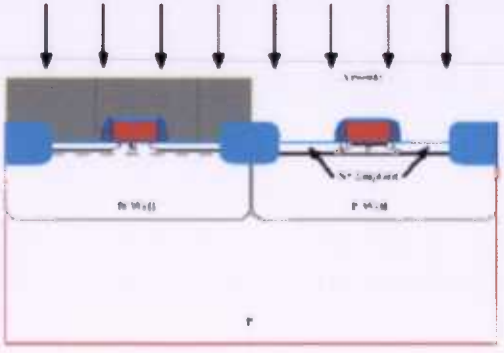


- **Sidewall formation:**
Anisotropic etching leaves behind "sidewall spacers" along the sides of the polysilicon gates.

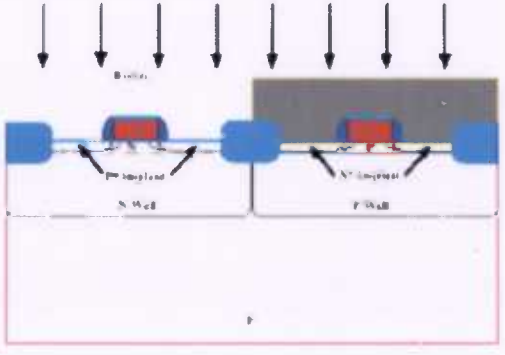


Deep Source & Drain Formation

CDEEP
IIT Bombay

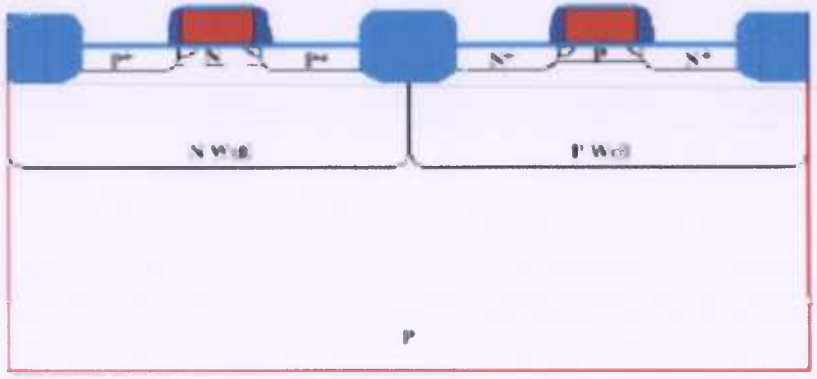


• **NMOS Deep Source/Drain formation:** Mask #9 protects the PMOS devices. An As+ implant forms the NMOS source and drain regions ("deep" = where the silicide contacts will form). Typical conditions are 2 - 4 x 10^{15} cm^{-2} @ 75 KeV.

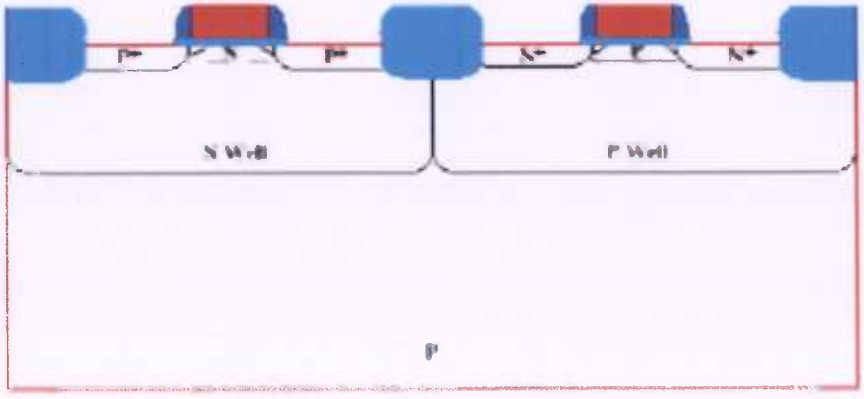


• **PMOS Deep Source/Drain formation:** Mask #10 protects the NMOS devices. A B+ implant forms the PMOS source and drain regions. Typical conditions are 1 - 3 x 10^{15} cm^{-2} @ 50 KeV.

Source & Drain Contact windows



• **Final anneal**: High temperature drive-in activates the implanted dopants and diffuses junctions to their final depths. Typical conditions: 30 min. @ 900C or 1 min. RTA at 1000C.



• **Contact formation:**
Unmasked oxide etch (HF dip) opens regions where contacts will be made to the Si and polysilicon.