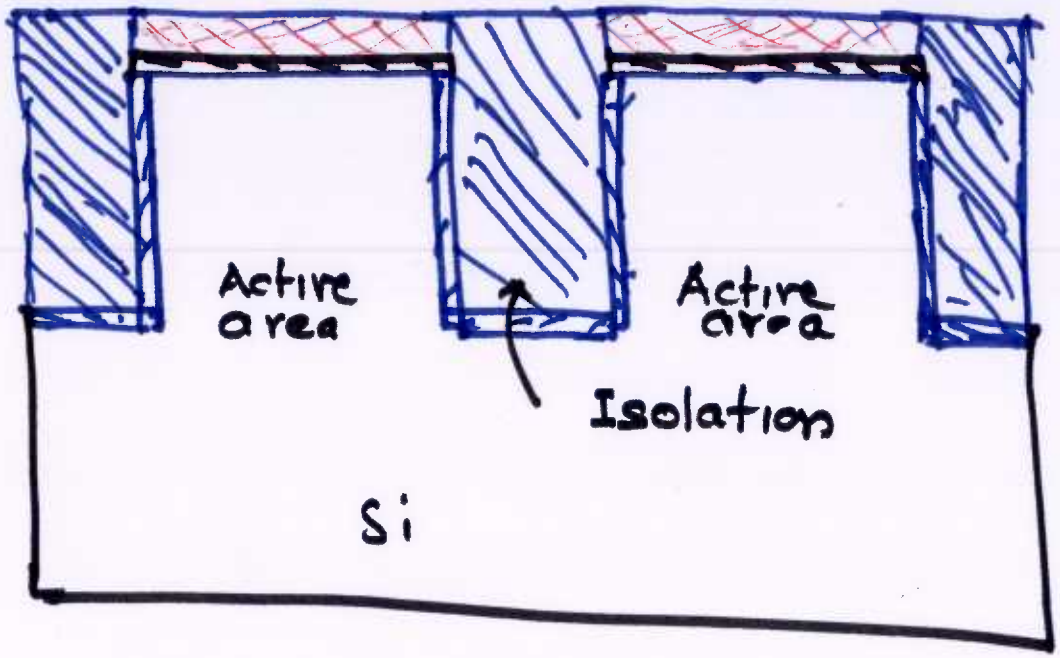
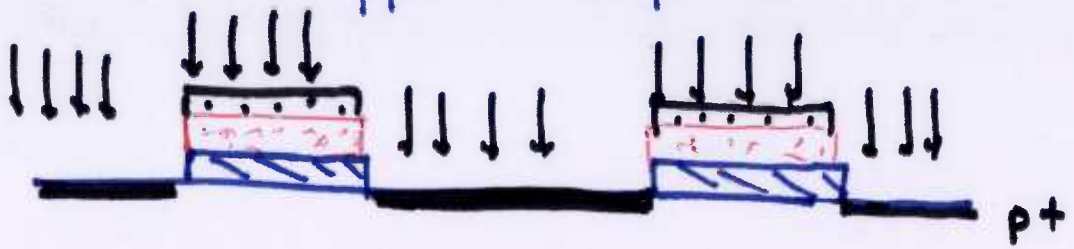
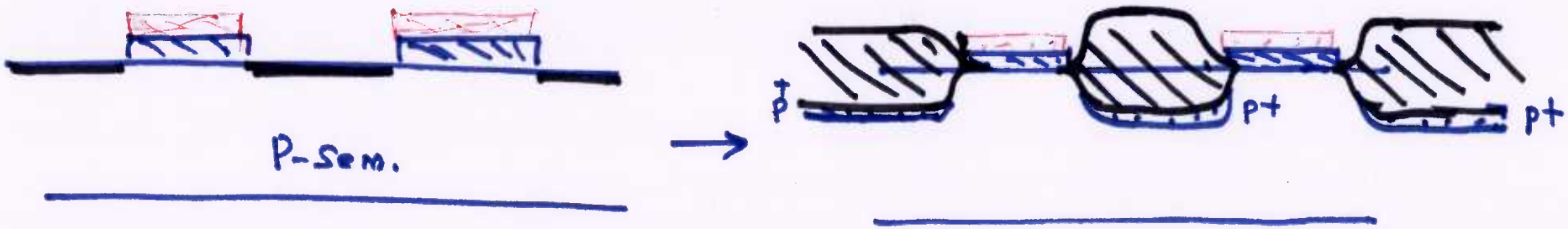


Recessed Trenched Oxide Isolation (STI)

Channel Stopper Implant



LOCOS PROCESS after Implant & removal of Resist.



$$V_{TF} = 2\phi_F + \phi_{ms} - \frac{Q'_{ox}}{C'_{ox}} - \frac{Q'_B}{C'_{ox}}$$

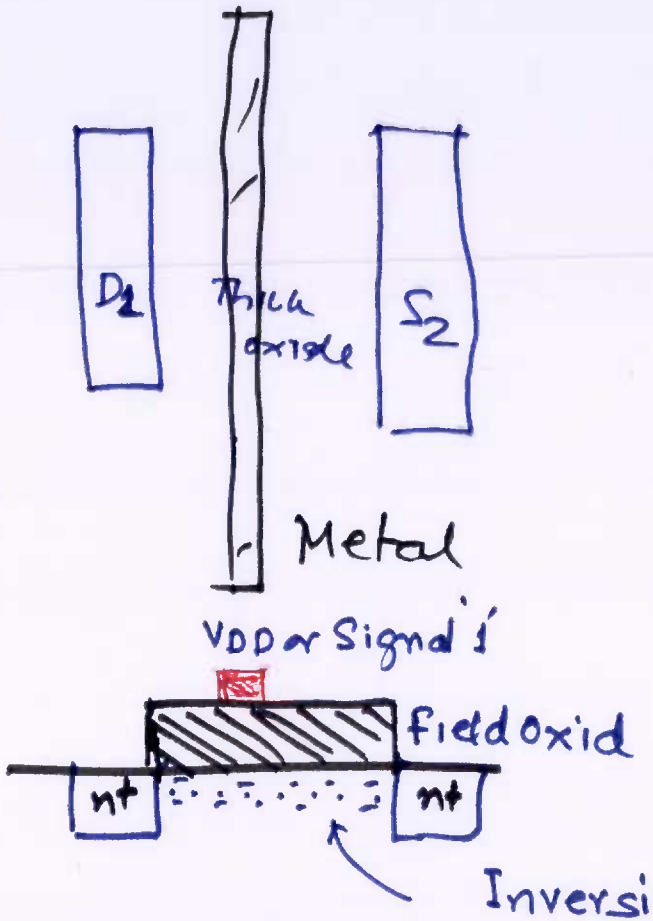
$$\therefore \Delta V_{TF} = -\frac{Q_{implant}}{C'_{ox}}$$

$$Q'_B = Q_B + Q_{implant}$$

$$Q_B = +q\, N_A x_{dmax} \quad \text{(P-Sub)}$$

$$V_{TF} = V_{TFO} + \Delta V_{TF}$$

$$C'_{ox} = \frac{\epsilon_{ox}}{t_{FOX}}$$


D2
Thick oxide
S2
Metal
VDD or Signal '1'
Field oxid
n+
n+
Inversion Channel
due FOX Inversion

NMOS :

CMOS Process steps

Acknowledgements

Most of the PPTs used here are taken from
Work of Prof. Jim Plummer of
Stanford University .

His book on "Silicon VLSI Technology" is being used as one of the Text Books for the Course of

EE 669:VLSI TECHNOLOGY

Similar slides are also available from the course PPTs
of VLSI Technology, a Graduate Course offered by Ms. Hoyt
At
Massachusetts Institute of Technology, Cambridge, USA
--------A.N.Chandorkar, IIT Bombay, Mumbai, INDIA
July to November 2014

Standard 16-Mask CMOS Process

2005 International Technology Roadmap for Semiconductors (ITRS)

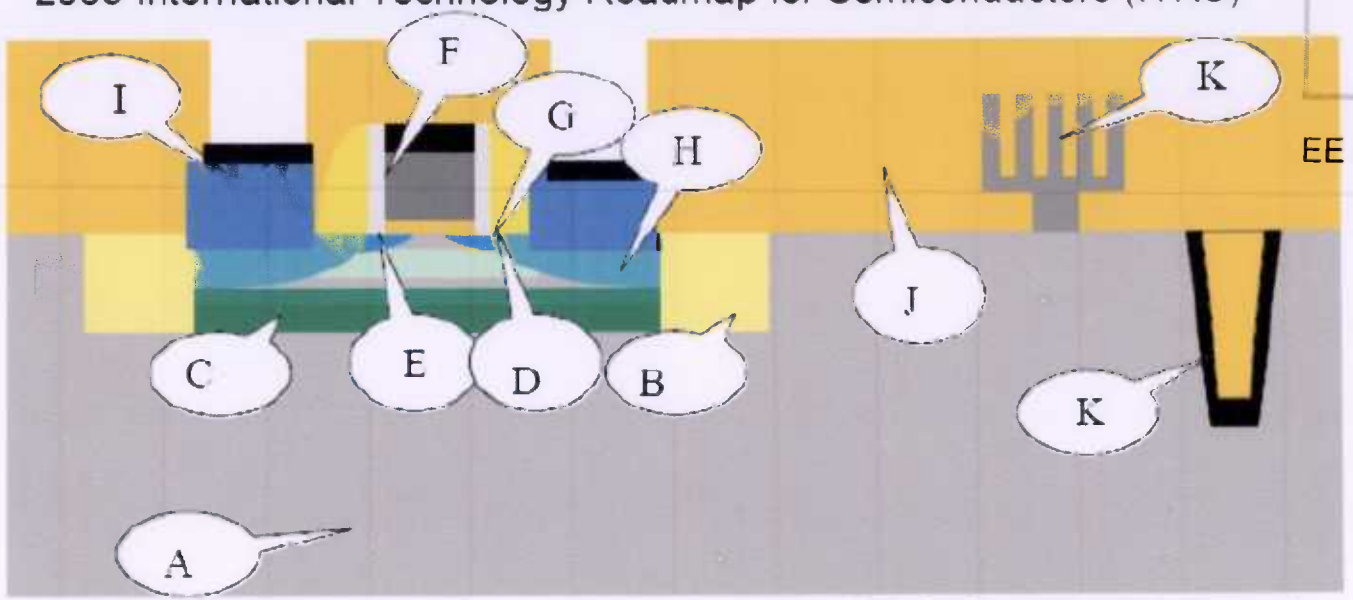


Figure 55 Front End Process Chapter Scope

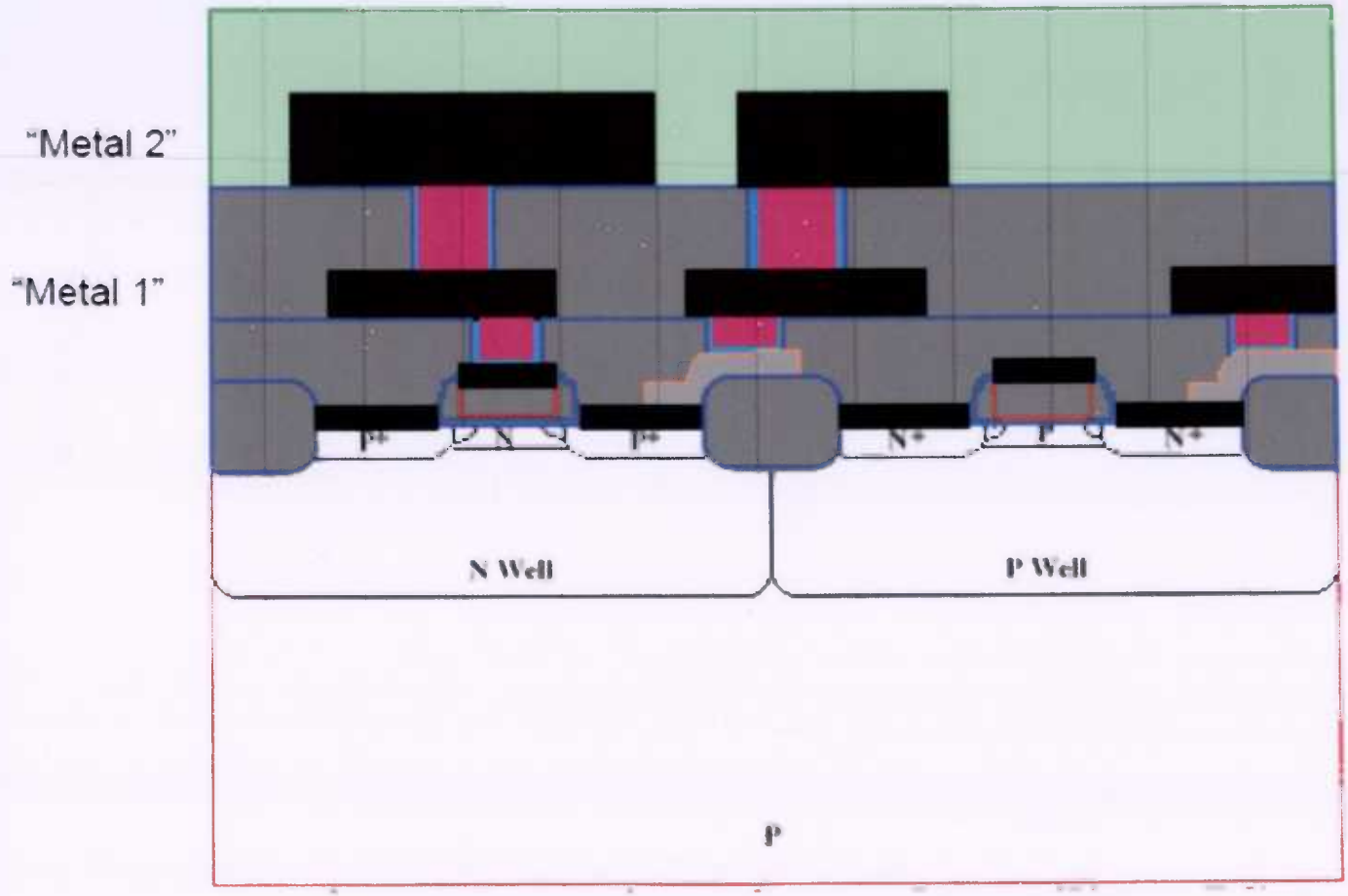
From "Front-end Processes" (FEP) Chapter, Downloaded 9/5/2006 from

http://www.itrs.net/Links/2005ITRS/FEP2005.pdf

Overall Structure of CMOS

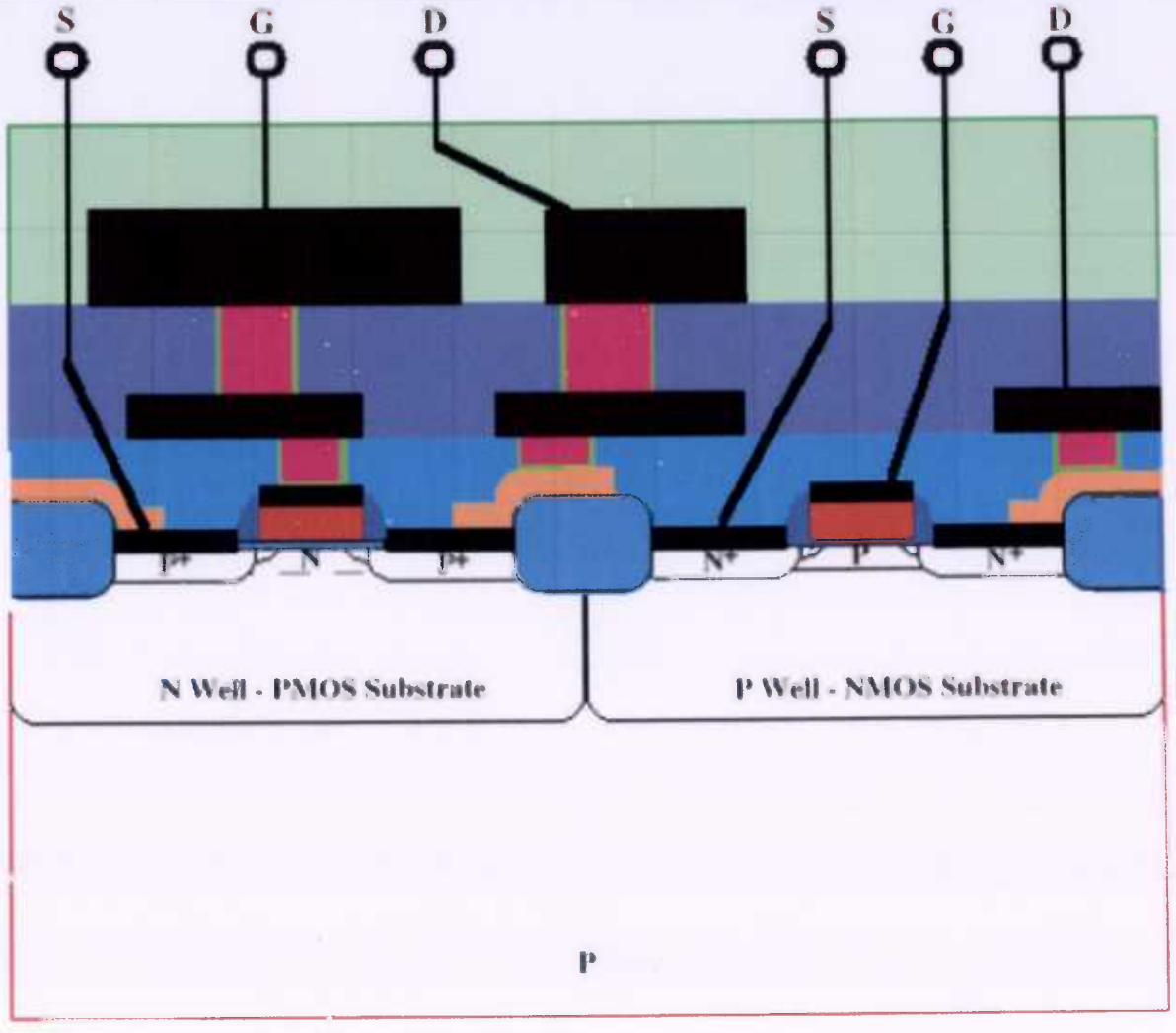
CDEEP
IIT Bombay

Schematic Cross Section of a Modern Silicon IC



(only two levels of wiring shown, for simplicity)

Two Level Metal Interconnect CMOS



- Final result of the process flow described here.

Step-I :"Active Area" Processes

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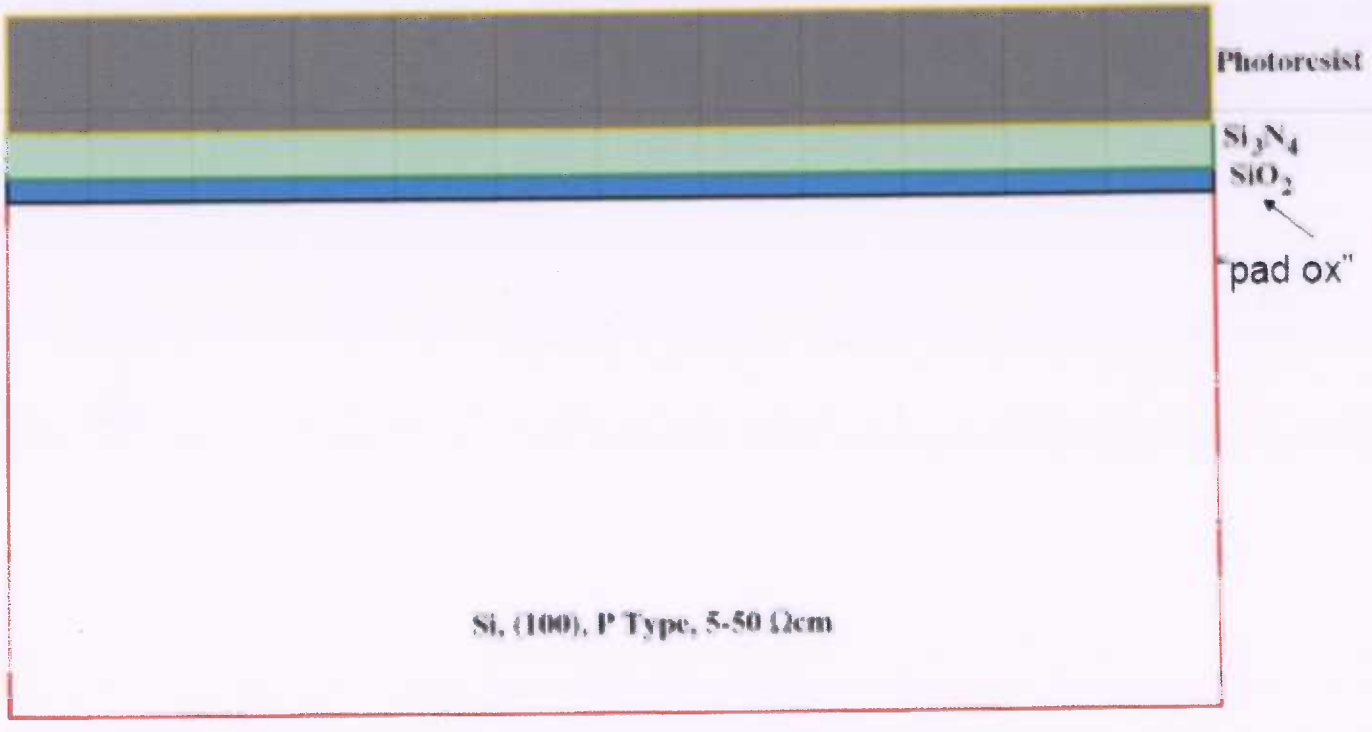
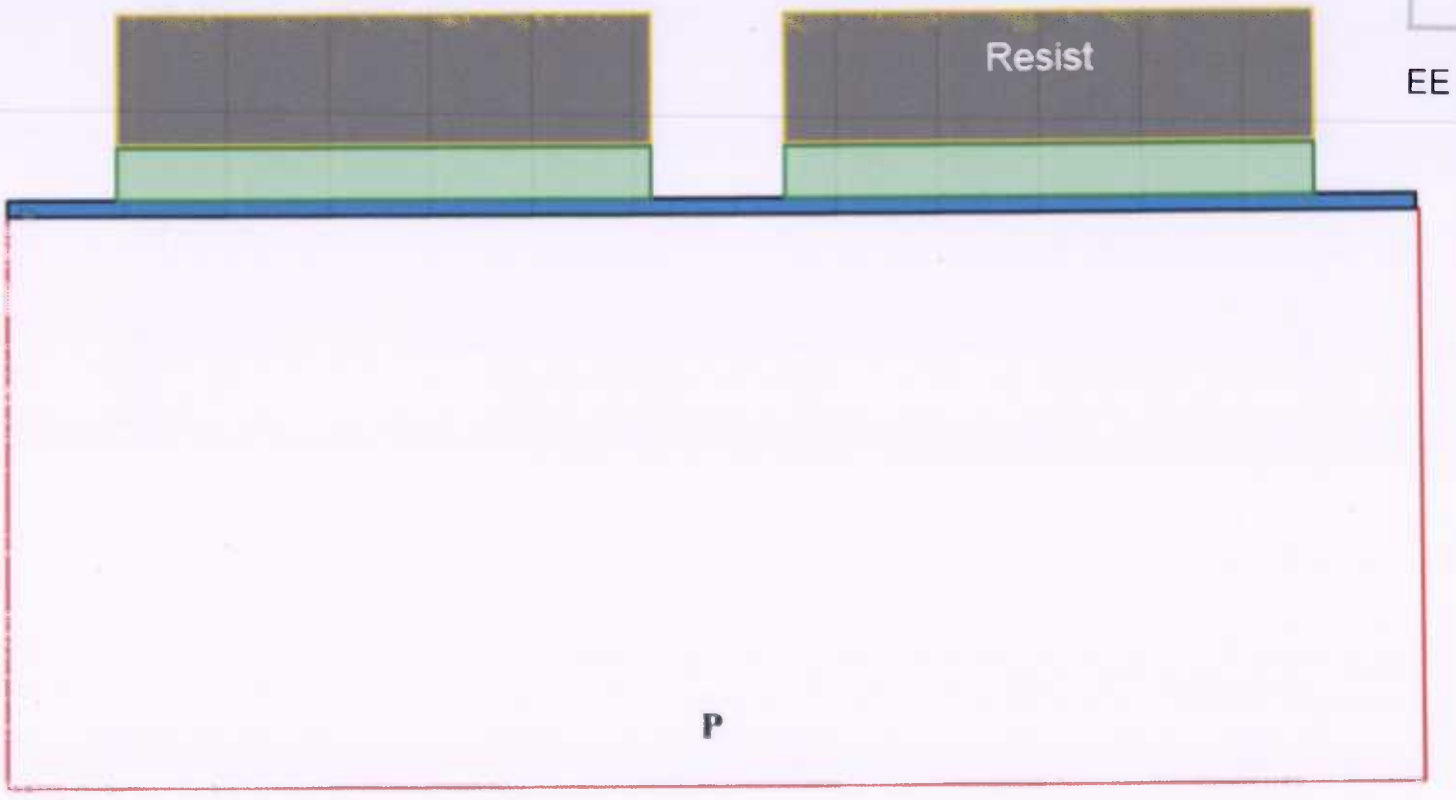
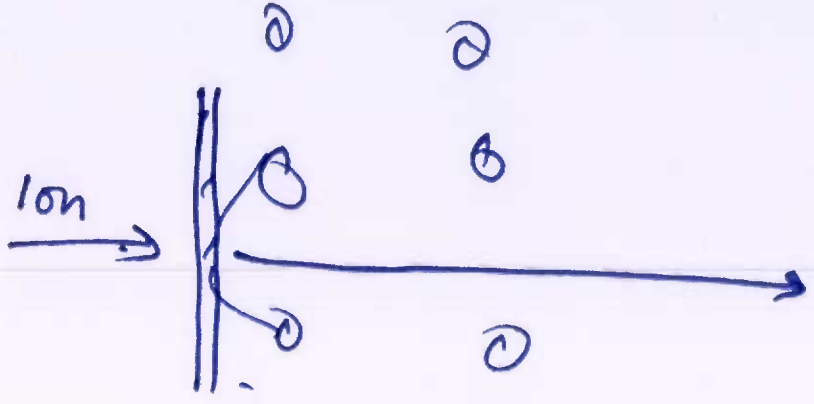


- Substrate: moderately high resistivity, (100) Si, p-type
- **Active region formation**: wafer cleaning, thermal oxidation (~40 nm), silicon nitride deposition (LPCVD) ~ 80 nm, photoresist coat (~0.5 - 1 micron)
- LPCVD Si_3N_4 is under tensile stress; compressive stress of thermal SiO_2 helps to balance this to reduce the stresses in the substrate (defect formation)

Active Area Delineation



• Mask 1 patterns the resist. The nitride is then dry etched to protect the active areas.


Ion
Channeling

LOCOS and P-well creation

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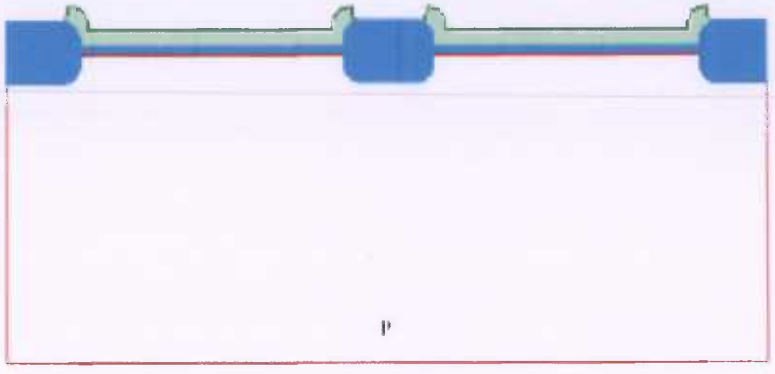
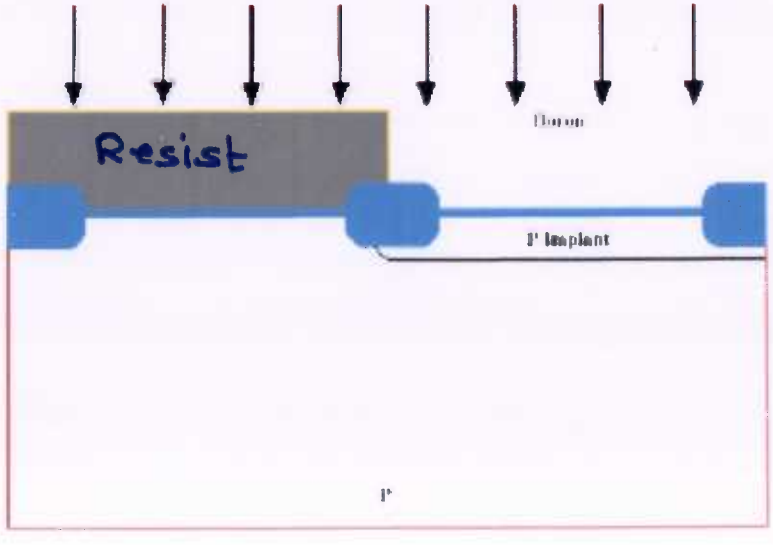


• **LOCOS**: after resist stripping the field oxide is grown using a Local Oxidation of Silicon process. Typical conditions are 1000°C, 90 min. in Steam ==> 0.5 micron oxide

Wet

Strip Nitride layer.



• **P Well Formation:** Mask #2 blocks a B+ ion implant to form the wells for the NMOS devices. Typical conditions are 10^{13} cm^{-2} @ 150 to 200 KeV (to yield final well concentration of ~ 10^{17} cm^{-3}).

PPR → Clear field Mask

P-well Mask