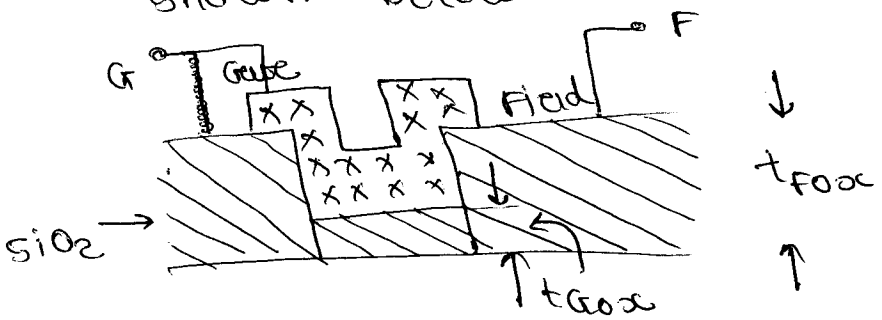
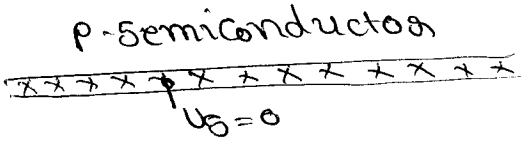
FABRICATION OF SILICON VLSI CIRCUITS USING THE MOS TECHNOLOGY

Model Problems

(1) N-type impurities are diffused in a p-wafer such that, n-layer is uniformly doped and junction depth is $x_j = 0.15$ μm. When one monitors sheet resistance, we obtain $\rho_S = 100$ ohms/□. Evaluate donor concentration if $\mu_n = 1300$ cm²/V.sec. ($q = 1.6 * 10^{-19}$ C).

(2) A Test structure in a CMOS process is shown below.





▨ - oxide ; ▩ - metal

(Figure : 1)

There are two capacitors observe here. One related to Gate oxide with thickness t_{Gox} and other one is due to Field oxide with thickness t_{Fox}.

The area of Gate capacitance is 4 μm² and field oxide capacitance is 25 μm².

Following were process steps :

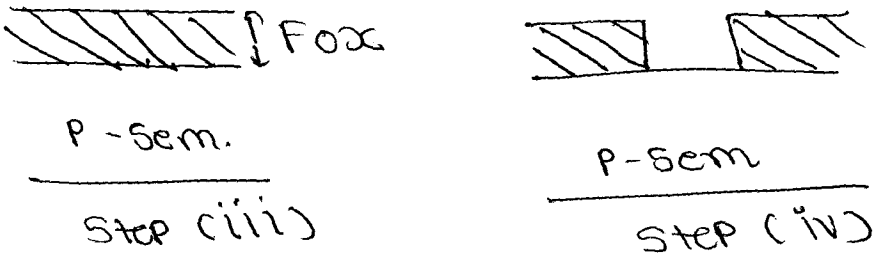
(i) Starting wafer is <100> oriented Silicon substrate with doping $5 * 10^{15}$/cc with Boron.

(ii) Before oxidation wafers were given RCA clean.

(iii) Field oxidation was performed with following sequence

(a) Dry oxidation : Temp = 1100°C, time = 2 hrs.

(b) Wet oxidation : Temp = 1150°C, Time: 110 minutes



Step (iii)

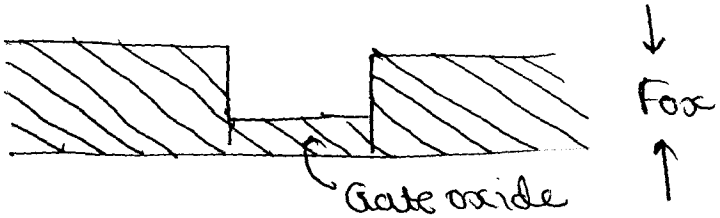
Step (iv)

(iv) Using a mask and lithography technique window in Fox opened which has area of 2 μm x 2 μm. In this area we shall create gate-oxide.

(v) Wafers were given RCA clean and wafers were loaded in the oxide furnace with process cycle as

(a) Dry oxidation: Temp = 950°C

time = 90 minutes



P-Semiconductor

Step (v)

(vi) wafers were RCA cleand and Aluminium film was evaporated on both sides of the wafers.

(vii) Using Scond mask (metal mask) and doing lithography, we realize two capacitors. one with Gate oxide and other with Fox.

For process standardisation, we monitor the two capacitances and get HF CV plots. Draw CV for both and mark V_{Tgate} and V_{TFox}.

The analytical V_{TS} were evaluated using data.

(1) $\phi_{ms} = 0$ (2) $Q_{ox} = 0$ (3) $2\phi_f = 0.6SV$

(4) $K_{ox} = 3.9$ (5) $K_{Si} = 12$ (6) $q = 1.6 * 10^{-19} C$

(7) $\varepsilon_0 = 8.85 * 10^{-14}$ F/cm^2 (8) $K = 1.38 * 10^{-23}$ J/^{0}K

→ In mut-shell evaluate V_{Tgate} and V_{TFox}. Assume $X_{dmax} = 0.4$ µm.

(3) A boron doped crystal pulled by the Czochalski technique is required to have a resistivity of 8 Ω cm. when half the crystal is grown.

Assuming that a 90 gm pure Silicon charge is used, how much 0.01 Ω.cm boron doped Silicon must be added to the melt? For this crystal, plot resistivity as a function of the fraction of the melt solidified. Assume $k_0 = 0.8$ and the hole mobility $\mu_p = 550\ cm^2/V.sec$

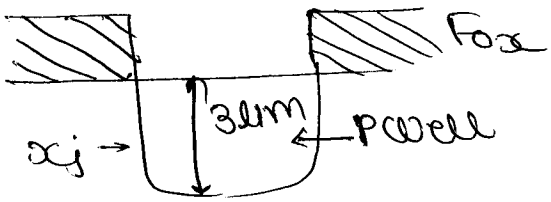
(4) An X-ray exposure system uses photons with an energy of 1.5 KEV. If the separation between the mask and wafer is 22 μm, Estimate the diffraction limited resolution that is achievable by this system.

(5) A Silicon wafer is covered by an SiO_2 film 0.35 μm thick.

(a) What is the time required to increase thickness by 0.5 μm by oxidation in H_2O at 1250°C?

(b) Repeat for oxidation in dry O_2 at 1200°C.

(6) In a typical CMOS process, one needs to create a p-well in n-substrate. p-well is used for nMOS transistors and substrate which is n-type is used for making pMOS devices.



N-Semiconductor

Deep p-well is about 3 μm deep for old 1 μm CMOS process. p-well is therefore created by diffusion technique with 2 steps process.

→ Initial substrate concentration is $N_d = 7 * 10^{15}$ /cc.

(i) Predeposition : constant source diffusion at

(a) Temperature = ??

(b) Time = ??

(c) Impurity Source = Boron

→ Measurements after predeposition gives surface concentration $N_0 = 2 * 10^{20}$ /cc

(ii) After predeposition, the grown Borosilicate glass is Etched out. Wafers were cleaned and loaded for Drive-in in the furnace.

Drive-in Temp = 1100°C

Drive in time = 9?.

Sheet resistance measurement gives $R_S = 65$ ohms/□. The junction depth measurement gives $x_j = 3?$ μm

You help the lab-engineer to evaluate

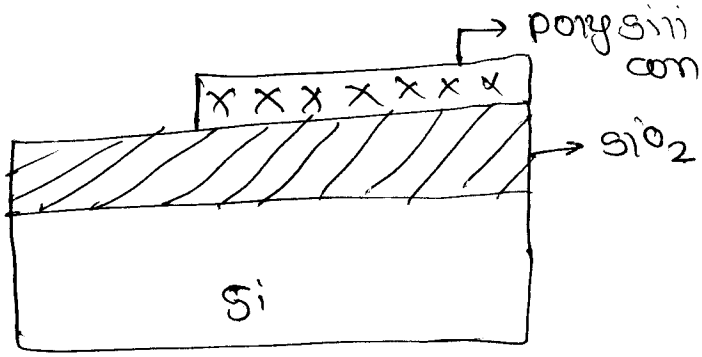
(A) Predeposition temperature

(B) Predeposition time

(C) Junction depth and Impurity Density after Predeposition.

(D) Drive in time

(7) A resistor for an Analog IC is made using a layer of deposited polysilicon of 0.4 μm thick, as shown below.



→ (a) The doping the polysilicon is $0.5 * 10^{16}$ /cm³. The carrier mobility $\mu = 100\ cm^2/Vsec$ is low because of scattering at grain boundaries. If the resistor has L = 80 μm & W = 15 μm. what is the resistance in ohms?

(b) A thermal oxidation is performed on the polysilicon for 2 hours at 900°C in H_2O.

Assuming B/A for polysilicon is 2/3 that of <111> silicon, what is the polysilicon thickness that remains. (7)

(c) Assuming that all of the dopant remains in the polysilicon (i.e does not segregate to oxide), what is the new value of the resistor in (a). Assume the mobility does not change.

(8) In a CMOS process, Tungsten is deposited for creating plugs in Vias, using sputtering process. Sputtering allows Argon ions to acquire energy of E which is due to cathode - Anode voltage of 100 V.

Threshold Energy Eth for sputter process of tungsten by Argon ions. is = 33 EV

Internal energy (sublimation Energy) is 191 Kcal/mol.

Evaluate the sputter yields what does it signify? Given $Z_W = 74$; $Z_{Ar} = 18$; $1 \frac{Kcal}{mol} = 0.0434$ EV/mol. Avagadro's no. = $6.022 * 10^{23}$/mol

(9) In a projection lithographic system, we have been using a light source with i-line wavelength of 365 nm The depth of focus DOF for this lense system is ± 0.35 lm The constant K_2 is DOF expression can be taken as 0.5. What is the resolution of

two lines possible in the system under use. Sketch intensity pattern for this case.

(10) A Boron Implant is carried out in Silicon which is coated with Si_3N_4 film. The energy of implant is 40 keV which allows peak concentration of dopant profile occuring at interface of Si_3N_4 film and Silicon. This process allows masking of impurities to the tune of 6 Nine's. You can take Rp of Boron in Si_3N_4 as 1.62 of Rp in Silicon. Evaluate thickness of Si_3N_4 film.

(11) A p-type (boron) diffusion is performed as follows:
Pre-dep: 30 minutes, 900°C, Solid solubility
Drive-in: 60 minutes, 1000°C

(a) What is deposited Q?
(b) If the substrate is doped $1.5 * 10^{15} cm^{-3}$ phosphorus, what is x_j.
(c) What is sheet resistance of the diffused layer?

(12) A $1.5 * 10^{14} cm^{-2}$ phosphorus implant through a 200 nm SiO_2 mask layer is performed to the peak concentration is at the silicon/SiO_2 interface. An anneal is then performed for 32 min

at 950°C. Calculate the location of the junction with the substrate doped at $1 * 10^{19}$ cm^{-3}. Assume no diffusion in the masking layer and ignore any segression effects. Assume the same range statistics for SiO_2 and Si.

(13) Calculate the deposition rate for a small planar surface evaporation source in which $\theta_i = 30°$, $\theta_k = 45°$, the evaporation rate is $1 * 10^{-3}$ gm sec^{-1}, the distance from the source to the wafer is 6 cm, and the density of the material being deposited equal 5.5 gm cm^{-3}.

(14) In a certain process, it is desired that the pitch of metal lines be equal to or less than 1.2 μm (the pitch equals one metal line width plus one spacing between metal lines, measured at top of features). Assume that the metal line width and spacing are equal (that is 0.6 μm each). The height of such structures is also 0.6 μm and the minimum lithographic dimension is 0.3 μm.

(a) What minimum degree of anisotropy is needed in an etch process in order to produce such a structure?

(b) What minimum pitch could be obtained for such a structure with wet etching? (10)
(Again with minimum lithograph dimension of 0.3 μm, thickness of 0.6 μm and equal metal width and spacing.)

* Reference :

(1) Silicon VLSI Technology
James D. Plummer, Michael D. Deal, Peta B. Griffin.