1. Segmentation unit allows segments of _____ size at maximum.
   a) 4Gbytes  b) 6Mbytes  c) 4Mbytes  d) 6Gbytes

2. If _____ input pin of 80386 if activated, allows address pipelining during 80386 bus cycles.
   a) BS16  b) NA  c) PEREQ  d) ADS

3. Virtual Mode Flag bit can be set using ____ instruction or any task switch operation only in the _____ mode
   a) IRET, Virtual b) POPF, Real c) IRET, protected d) POPF, protected

4. The interrupt vector table of 80386 has been allocated ______ space starting from ______ to ______.
   a) 1Kbyte, 00000H, 003FFH  b) 2Kbyte, 10000H, 004FFH  c) 3Kbyte, 01000H, 007FFH  d) 4Kbyte, 01000H, 009FFH

5. The ___ bit decides whether it is a system descriptor or code/data segment descriptor.
   a) P  b) S  c) D  d) G

6. A new signal group on the 80486 is the ______.
   a) PARITY  b) DP0-DP3  c) PCHK  d) all

7. _____ is used to control the cache with two new control bits not present in the 80386 microprocessor. What are the bits used to control the 8K byte cache?
   a) CR0, CD, NW  b) CR0, NW, PWT  c) Control Register Zero, PWT, PCD  d) none

8. To prevent another master from taking over the bus during a critical operation, the 486 can assert its _____ signal.
   a) LOCK# or PLOCK#  b) HOLD or BOFF  c) HLDA  d) HOLD

9. 80386 support which type of descriptor table from the following?
   a) TDS  b) ADS  c) GDS  d) MDS

10. 80386 support overall ___ addressing modes to facilitate efficient execution of higher level language programs.
    a) 9  b) 10  c) 11  d) 12
Key:
8.1 A 8.2 B 8.3 C 8.4 A 8.5 B 8.6 D
8.7 A 8.8 A 8.9 C 8.10 C