1. Access time is faster for
   a) ROM     b) SRAM     c) DRAM

2. In 8279 Strobed input mode, the control line goes low. The data on return lines is strobed in the ____.
   a) FIFO byte by byte   b) FILO byte by byte   c) LIFO byte by byte
   d) LILO byte by byte.

3. ____ bit in ICW1 indicates whether the 8259A is cascade mode or not?
   a) LTIM=0   b) LTIM=1   c) SNGL=0   d) SNGL=1

4. In 8255, under the I/O mode of operation we have ___ modes. Under which mode will have the following features
   i) A 5 bit control port is available.
      ii) Three I/O lines are available at Port C.
   a) 3, Mode2   b) 2, Mode 2   c) 4, Mode 3   d) 3, Mode 2

5. In ADC 0808 if _______ pin high enables output.
   a) EOC     b) I/P0-I/P7     c) SOC     d) OE

6. In 8279, a scanned sensor matrix mode, if a sensor changes its state, the ___ line goes ____ to interrupt the CPU.
   a) CS, high    b) A0, high     c) IRQ, high   d) STB, high

7. In 8279 Status Word, data is read when ________ pins are low, and write to the display RAM with __________ are low.
   a) A0, CS, RD & A0, WR, CS.     b) CS, WR, A0 & A0, CS, RD
   c) A0, RD & WR, CS     d) CS, RD & A0, CS.

8. In 8279, the keyboard entries are debounced and stored in an _________, that is further accessed by the CPU to read the key codes.
   a) 8-bit FIFO   b) 8-byte FIFO     c) 16 byte FIFO   d) 16 bit FIFO

9. The 8279 normally provides a maximum of _____ seven segment display interface with CPU.
   a) 8    b) 16    c) 32    d) 18

10. For the most Static RAM the write pulse width should be at least
    a) 10ns   b) 60ns   c) 300ns   d) 1µs

11. BURST refresh in DRAM is also called as
    a) Concentrated refresh   b) distributed refresh   c) Hidden refresh   d) none

12. For the most Static RAM the maximum access time is about
    a) 1ns   b) 10ns   c) 100ns   d) 1µs

13. Which of the following statements on DRAM are correct?
    i) Page mode read operation is faster than RAS read.
    ii) RAS input remains active during column address strobe.
    iii) The row and column addresses are strobed into the internal buffers using RAS and CAS inputs respectively.
    a) i & iii   b) i & ii    c) all   d) iii

14. 8086 microprocessor is interfaced to 8253 a programmable interval timer. The maximum number by which the clock frequency on one of the timers is divided by
    a) $2^{16}$   b) $2^{8}$   c) $2^{10}$   d) $2^{20}$
15. 8086 is interfaced to two 8259s (Programmable interrupt controllers). If 8259s are in master slave configuration the number of interrupts available to the 8086 microprocessor is
a) 8    b) 16    c) 15    d) 64
Key:
3.1 B 3.2 A 3.3 C 3.4 B 3.5 D 3.6 C
3.7 A 3.8 B 3.9 B 3.10 B 3.11 A
3.12 C 3.13 C 3.14 A 3.15 D