CAD for VLSI Design - II

Lecture 1

V. Kamakoti and Shankar Balachandran

About the course

- Advanced Digital Fundamentals
  - Transistor Theory
  - Arithmetic Circuits Design
  - Pipelining fundamentals
  - Case study of a pipelined superscalar processor
  - ASIC Design flow

The Course Starts Here

Transistor Theory

History: Transistor Revolution

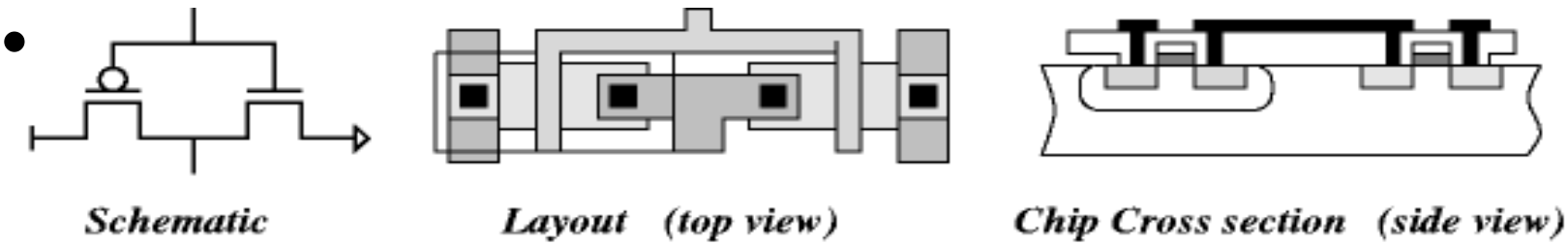
- 1947: Transistor by J. Bardeen, W. Brattain at Bell Labs.
- 1949: Bipolar transistor by W. Shockley.
- 1956: First bipolar digital logic gate by Harris
- 1958: First monolithic IC by Jack Kilby at Texas Instruments.
- 1960: First commercial logic gate IC from Fairchild.
- 1962: TTL – the *first IC revolution*
- 1974: ECL – first sub-nanosecond digital gates.

Tech.	Year	Approx. # trans./chip	Typical Products
Devices	1950-60	1	Transistors and diode
SSI	1960-65	10	Logic gates, latches, etc.
MSI	1965-70	100 - 1K	Counters, adders, etc.
LSI	1970-80	1K - 20K	8-bit µProc., ROM, RAM, …
VLSI	1980-85	20K - 500K	16-bit µProc., peripherals, …
ULSI	1986-	> 500K	32-bit µProc., DSPs, ASICs, …

MOSFET Technology

- 1925: Basic principle behind MOSFETs (IGFET) – independently proposed by J. Lilienfeld (Canada) in 1925 and O. Heil (England) in 1935.
- 1963: CMOS gate – F. Wanlass and C. Sah. Plagued with manufacturing problems.
- 1960's: PMOS for calculators.
- 1972: Intel 4004 – the *second IC revolution*. NMOS used for speed.
- 1980s: CMOS – dominant technology of the information age because of lower power and ease of design.
- BiCMOS, SiGe, GaAs, …
- Cu interconnect, low-K dielectric, SOI, …

CMOS Technology

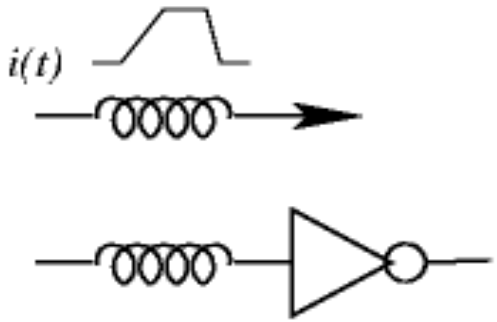
- CMOS – Complementary Metal Oxide Semiconductor.
- MOSFET – a sandwich structure of Metal, Oxide and Semiconductor. Modern processes use *polysilicon* instead of metal for gate - originally called IGFET.
- 

Technology Roadmap: ITRS 2001

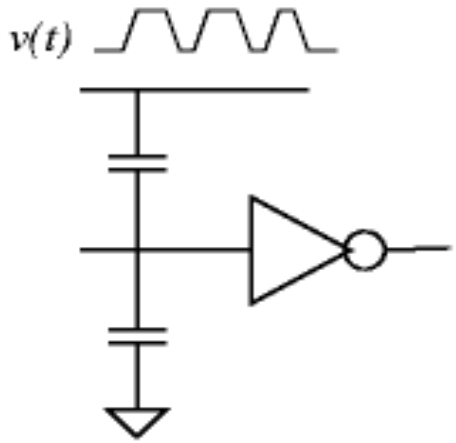
Year	2001	2003	2006	2010	2013	2016
Feature size (nm)	130	90	53	32	22	16
Mtrans/cm²	38	61	122	309	617	1235
DRAM bits (Gbits)	0.512	1	2	8	32	64
Chip size (mm²)	280	280	280	280	280	280
Signal pins / chip	1024	1024	1024	1280	1408	1472
Power/GND pins/chip	2048	2048	2048	2560	2816	2944
Clock rate (GHz)	1.7	3.1	5.6	11.5	19.3	28.8
Wiring levels	7	8	9	10	10	10
Power supply (V)	1.1	1.0	0.9	0.6	0.5	0.4
High-perf power (W)	130	150	180	218	251	288
Battery power (W)	2.4	2.8	3.5	3.0	3.0	3.0

Reliability: Noise in Digital ICs

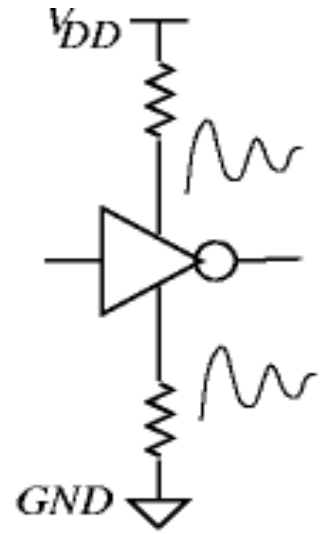
- Noise – unwanted variations of voltage and currents at nodes in a logic circuit.
- Most noise in a digital system is internally



Inductive coupling



Capacitive coupling

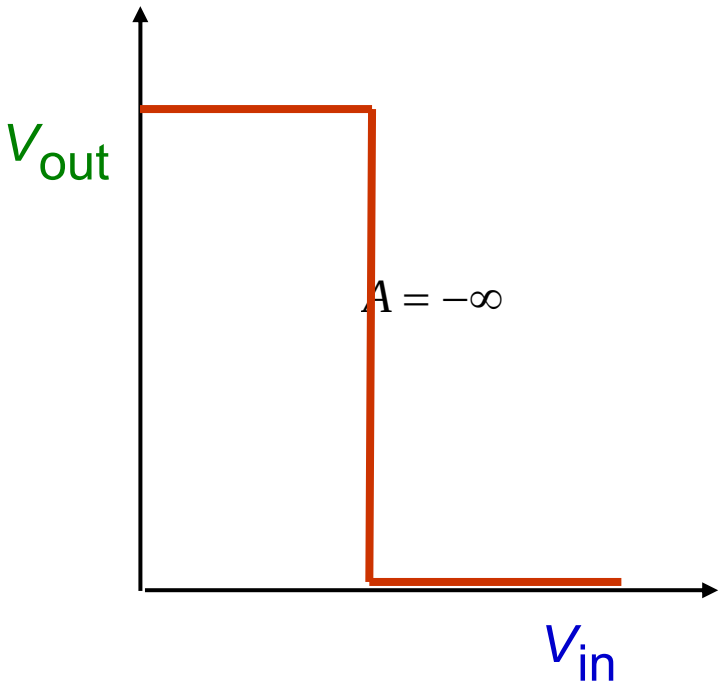


Power & Ground noise

Noise Immunity

- *Noise immunity* expresses the ability of the system to process and transmit information correctly in the presence of noise ⇨ *reject a noise source instead of overpowering it*
- For a given set of noise sources, the minimum signal swing necessary for the system to be operational can be derived.
- The signal swing (and the noise

The Ideal Inverter



Gain in the transition region: $A = -\infty$

$R_{in} = \infty$

$R_{out} = 0$

$V_M = V_{dd}/2$ (middle of the logic swing)

$NM_H = NM_L = V_{dd}/2$

Fanout = ∞

Questions and Answers

Thank You