Course Objectives

- The course has two parts
  - CAD for VLSI Design - 1
    - Introductory course
    - Different stages in VLSI Design flow
    - Front-end VLSI Design
    - FPGA Design flow
  - CAD for VLSI Design - 2
    - Transistor level design issues
    - Logic Synthesis and Static Timing Analysis
    - High-speed circuits and processor architectures
    - ASIC Design flow
CAD for VLSI Design - I

• Structure of Theory part
  – Introduction to VLSI Design Flow
  – CMOS Circuit and Logic Design
  – Front-end VLSI Design using Verilog
  – FPGA Design flow

• Abbreviations
  – CAD - Computer Aided Design
  – VLSI - Very Large Scale Integration
  – CMOS - Complimentary Metal Oxide Silicon
  – FPGA - Field Programmable Gate Arrays
  – Much more to come :-)

CAD for VLSI DESIGN I
CAD for VLSI Design - I

- **Structure of the Lab part**
  - Simple designs to be coded in Verilog HDL
  - Some designs to be taken through the FPGA Design flow
    - For details on access or procurement of the necessary FPGA tools and boards contact
      - Dr. V. Kamakoti,
      - Department of Computer Science and Engineering
      - Indian Institute of Technology, Madras
      - Chennai - 600 036, India
      - Email: kama@cs.iitm.ernet.in
CAD for VLSI Design - I
Course Starts Here

All The Best
Evolution Of CAD Tools

- Digital circuit design evolved over last three decades
- SSI – Small Scale Integration (Tens of transistors)
- MSI – Medium Scale Integration (Hundreds of transistors)
- LSI – Large Scale Integration – (Thousands of Transistors) - demanded automation of design process – CAD started evolving.
Evolution Of CAD Tools

- VLSI – Very Large Scale Integration – Tens of Thousands of Transistors – CAD Tools are inevitable
- VLSI chip design forced
  - Automation of process
  - Automation of Simulation based verification - replacing breadboard techniques – HDL development
  - Modular and Hierarchical techniques of design – a natural object orientation approach
CAD Terminologies

• HDL – Hardware Description Language
  – Describing a circuit to the computer
  – A programming language by all means
  – Concurrency constructs to simulate circuit behavior
  – Verilog and VHDL
  – Simulation for verification and Synthesis
  – Synthesizable constructs - RTL
CAD Terminologies

• RTL – Register Transfer Level
  – Specifying how the data flows between registers and how the design processes data
  – Registers store intermediate results
  – Logic between any two registers in a data flow determines the speed of the circuit

• Synthesis – Converting RTL to a set of gates and wires connecting them – Ambit of Cadence, Design Compiler of Synopsys, Precision of Mentor, Blast Fusion from Magma are some of the commercially available synthesis tools.
VLSI FPGA Design Flow

Front End

- Design Specification
- Behavioral Description
- RTL Description (HDL)
- Functional Verification And Testing
- Logic Synthesis and Tech. mapping

Back End

- Technology Netlist
- Placement
- Routing
- Bit stream
- Programming FPGA by Downloading the bit stream

CAD for VLSI DESIGN I
Questions and Answers
End of Lecture 1
Thank You