Digital Switching
Questions which can be asked in quizzes and examinations.

1. Draw a 4x4 crossbar network. Explain the mechanism to be used if there are only four row control lines and four column control lines, for controlling the individual crosspoints.

2. What is Paull's matrix? What are the conditions for valid Paull's matrix for unicast and multicast conditions?

3. State and prove Clos theorem for unicast switching network. Derive the conditions for strictly non blocking condition for k-way multicasting in Clos network. Give reasoning for validity of your conditions.

4. State and prove Slepian Duguid theorem. What is the maximum number of rearrangements required. Give all possible bounds on it using single chain search and dual chain search.

5. Derive the crosspoint complexity bound on recursively constructed strictly non-blocking clos network.

6. What is a wide-sense non-blocking network. Give an example. Prove that the example given by you is wide-sense non-blocking network.

7. Draw a schematic of 32x128 single stage time switch with read cyclic write acyclic configuration. Comment on the scheme if we create it using reach acyclic and write cyclic configuration.

8. Derive the condition when Cantor network is strictly non-blocking. Also find the crosspoint complexity of the strictly non-blocking Cantor network.

9. Define call congestion and time congestion. Intuitively explain which one of them will be lesser and why? Determine the relationship between call congestion and time congestion.

10. Define wide-sense non-blocking, strict sense non-blocking, re-arrangeably non-blocking, and blocking nature of a switching network.

11. For recursively constructed strictly non-blocking Clos network, determine crosspoint complexity.

12. Draw a wide-sense non-blocking network of size 4x4. Prove that is wide-sense non-blocking.

13. For 9x9 switch built using 3x3 switching elements, draw a rearrangeably non-blocking switch. Draw the following connections so that if we try to setup 2→2' in the end, it is blocked. 1→8', 3→7', 4→1', 5→6', 6→5', 7→4', 8→9', 9→3'.

14. Show the re-arrangement procedure on Paull's matrix after which 2→2' can be setup.

15. Draw a 32x32 time switch schematic using RAM with asynchronous write and synchronous read.

16. Mention in which half of the clock,
1. Write happens in speech memory.
2. Write happens in control memory.
3. Read happens in speech memory.
4. Read happens in control memory

17. What are the sizes of speech memory and control memory?

18. In a 16x16 packet switch made using crossbar, if 12 packets contend for an output, only 8 packets can move to output queue. No packet is lost in this system.

1. The switch is
   1. fully output queued switch
   2. fully input queued switch
   3. hybrid input and output queued switch
   4. none of the above.

2. The speed up factor is
   1. 16
   2. 12
   3. 1
   4. 8

3. The speed up factor switch to be fully output queued switch should be
   1. 16
   2. 12
   3. 1
   4. 8

19. In a fully input queued packet switch based on crossbar, when the packets which are unsuccessful in moving to an output, are dropped, what is the throughput for given input load $p$. Identify the range of input load $p$ for which, the strategy of dropping the backlogged packet will surely give better throughput performance that input queued switch where packets are not dropped. The throughput of input queued switch under full load conditions is $2 - \sqrt{2}$.

20. For an input queued switch under full load we define $A_m^i = $ packets destined for output $i$ moving to head of queue in slot $m$, $B_m^i = $ packet at the head of the queue, destined for output $i$ in slot $m$. The following relation holds.

21. $B_m^i = \max(0, B_{m-1}^i + A_{m-1}^i)$; $F_{m-1} = N - \sum_{i=1}^{N} B_m^i$ and

   $Pr(A_m^i = k) = \left( \frac{F_{m-1}}{N} \right) k \left( 1 - \frac{1}{N} \right)^{F_{m-1} - k}$. Assume packet transmission takes one slot, moving of packet from one position to another in the queue is instantaneous. Find the appropriate timing diagram showing $B_m^i$, $A_m^i$ and packet transmission. A possibility is shown in Fig. III-1.

22. Define a) Banyan network, b) Delta network. How self routing is achieved in Banyan network?

23. Define r-shuffle ($S_{rsq}$) of qr objects. Write both mathematical forms.
24. Prove \( S_{q,r}(S_{r,q})(i) = i \).

25. In a shufflenet with elementary switches of size \( a \times b \) and \( n \) stages, a packet is destined for \( d_{n-1}d_{n-2} \cdots d_0 \) from source \( s_{n-1}s_{n-2} \cdots s_0 \). If packet emanates at the output \( L_i \) of stage \( i \), where \( L_i = s_{n-i}a^{n-i-1} + \cdots + s_2a + s_1b^i + d_{n-i}b^{n-i-1} + \cdots + d_0 \).

26. Find the input \( L_i' \) of stage \( i + 1 \) to which, the packet will be routed.

27. Draw Cantor network. Derive the condition, and thus the crosspoint complexity, for it to be strictly nonblocking.

28. Explain the congestion control queuing models i.e., (i) blocking and (ii) delayed dial tone models, for the circuit switches. For the call blocking model i) derive the call blocking probability (\( P_B \)), ii) derive the average call processing delay, iii) derive the call throughput and task throughput. For the delayed dial tone delay model, derive the average call processing delay and average waiting time before the call processing starts.

29. Draw the 16x16 baseline and inverse baseline networks using 2x2 basic switching elements. Rearrange the basic switching elements, so that both gets transformed to 16x16 shufflenet. Show this by keeping the numeric identifier same while moving the 2x2 switching elements from one position to another.

30. Draw a T-S-T switch using cyclic write, acyclic read in first stage, and acyclic write, cyclic read in third stage. Use a cross bar of 4x4. Each input line has 32 voice slots in a frame. Draw all control memories and speech memories needed in this switch specifying their sizes. The switch should be strictly nonblocking.


32. Define time congestion and call congestion. Derive the relationship between them.

33. Draw and explain the operation of supermultiplexed time for 16 PCM streams; each carrying 30 voice channels.

34. Draw the crossbar switching network. Explain how the switch control will be implemented using minimum control lines so that all possible connections can be established.

35. Define blocking, strictly nonblocking and rearrangeably nonblocking switching network.

36. What is difference in functionality of
   1. Stateless proxy,
   2. transaction stateful proxy,
   3. call stateful proxy.

37. What other protocols are needed alongwith SIP for implementing a communication infrastructure? Explain the purpose of each one of them.

38. Explain how a call is setup between Alice and Bob using SIP proxies in their domain.

39. Why SIP proxies are needed?

40. The INVITE request is as follows

   INVITE sip:bob@biloxi.com SIP/2.0
   Via: SIP/2.0/UDP pc33.atlanta.com;branch=z9hG4bK776asdhds
Max-Forwards: 70
To: Bob <sip:bob@biloxi.com>
From: Alice <sip:alice@atlanta.com>;tag=1928301774
Call-ID: a84b4c76e66710@pc33.atlanta.com
CSeq: 314159 INVITE
Contact: <sip:alice@pc33.atlanta.com>
Content-Type: application/sdp
Content-Length: 142

(Alice’s SDP not shown)

Explain the purpose and meaning of each of the header fields.

41. What response codes are sent in the responses to various requests. Also mention the purpose of each of the category of codes.

42. What methods are permitted in the request message by RFC3261. Also mention the purpose of each method.

43. Define q-shuffle of qr objects.

44. Prove $a^n \times b^n$ shufflenet with a-shuffle as inconnection pattern between consecutive stages is a Delta network.

45. What is speedup factor? For implementing an output queued switch, what is the value needed?

46. Derive the expression for probability of call loss (call congestion) using Karnaugh’s approach for a three stage clos network.

47. Find the crosspoint complexity for a recursively constructed strictly non-blocking switch using Clos network.

48. State and prove Slepian-Duguid theorem.

49. Draw a strictly non-blocking TST switch. In first stage let there be four time switches. The input to each time be 16 time slots per frame. Mention explicitly all the speech as well as control memory sizes alongwith the word size used in them. Take WCRA time switch in first stage and WARC time switches in third stage. Show how slot 5 in switch 1 and slot 3 in switch 4 in stage 1 can be mapped to slot 3 in switch 4 and slot 5 in switch 1 respectively in stage 3, by putting appropriate content at appropriate locations in all the control memories.

50. Draw all possible states of a 2x2 switch in buffered delta network.

51. When $t_{pass}=0$, find the expression for $\tilde{p}_j = \text{probability that in step 3, a packet arrives at the input port a 2x2 switch in stage } j$.

52. When $t_{select}=0$, find the transition probabilities from the following switch state to all the states for a 2x2 switching element in stage $j$. Your answer should be consistent with your answer in prob I.A.

53. Derive the maximum achievable throughput in an input queued crossbar based packet switch.

54. If all the unsuccessful packets are dropped at the input ports, derive the throughput. In what range of arrival rate, this strategy should be used.

55. Draw the petrinet model for 2x2 switch in buffered delta network.

56. What are the boundry conditions for the computational procedure of buffered delta analysis?
3. Give the sequence (how) of the computation to be done to get the state probabilities in all stages.

4. How we find that the computation has converged?