Lecture 26: Etching and deposition

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1 Etching

Etching refers to the removal of material from the wafer surface. The process is usually combined with lithography in order to select specific areas on the wafer from which material is to be removed. Etching represents one way of permanently transferring the mask pattern from the photoresist to the wafer surface. The complementary process to etching is deposition (or growth), where new material is added. Unlike oxidation (or nitridation), where the underlying Si is consumed to form the oxide (nitride) layer, in deposition, new material is added without consuming the underlying wafer.

There are two main types of etching

1. Wet etching
2. Dry etching

1.1 Wet etching

In wet etching, the wafers are immersed in a tank of the etchant (mix of chemicals), as shown in figure 1. There is a chemical reaction between the wafer surface and the etchants that helps in material removal. Either a photoresist layer or a hard mask like oxide or nitride layer is used to protect the rest of the wafer. The time for etching depends on the amount and type of material that needs to be removed. KOH (potassium hydroxide) is a common etchant used to remove Si. Usually, 30% KOH solution is used, which has an etch rate of \(\sim 100 \mu m/hr\) at 90 °C. Thus, an entire 4” wafer, with thickness of 500 \(\mu m\), can be etched through in approximately 5 hours. The etch rate of Si (100) by 30 % KOH is shown in figure 2. After etching, the wafers are rinsed, usually in DI water, for removal of etchant and then finally dried.

Wet etching is used for removal of material from large areas (trench sizes > 3 \(\mu m\)). For smaller areas, where greater precision in removal of material is required, dry etch is preferred. The wet etching process is anisotropic i.e. the etch rate depends on the plane of the Si wafer, from which atoms are being

![Figure 1: Schematic of the wet etching process. A controlled portion of the wafer surface is exposed to the etchant which then removes materials by chemical reaction. Adapted from Fundamentals of semiconductor manufacturing and process control - May and Spanos.](image-url)
Figure 2: Etch rate of Si in KOH as a function of temperature. There is a non-linear increase in etch rate with increasing temperature. Typically, etching is carried out at 90 °C. Source [http://www.cleanroom.byu.edu/KOH.phtml](http://www.cleanroom.byu.edu/KOH.phtml)

removed. The etch rate for Si (110), in the same 30 % KOH, is shown in figure 3. Compared to Si(100) plane, figure 2 the rate is higher. This means that wet etching of Si(100) will produce a trapezoidal profile, with a specific angle of 54.74 deg, as shown in figure 4. Etching uniformity is important to get a uniform thickness over the entire wafer surface. This is usually determined by process conditions like etchant temperature, concentration, and agitation (using stirrers).

1.2 Etching challenges

There are some process challenges related to etching. These are common to both wet and dry etching, though they are more pronounced and harder to control in wet etching due to the higher rate of material removal, compared to dry etching.

1.2.1 Incomplete etch

In incomplete etch, the time is not sufficient for complete material removal. This is usually due to concentration or temperature not being sufficient. The concentration profile left behind is usually a rough surface, due to local variations in material removal, as depicted in figure 5.
Figure 3: Etch rate of Si(110) in KOH as a function of temperature. Compared to the etch rate for Si (100), see figure 2, the etch rate is higher. Source [http://www.cleanroom.byu.edu/KOH.phtml](http://www.cleanroom.byu.edu/KOH.phtml)

Figure 4: Anisotropic etching of Si by KOH. Because of the difference in the etch rates of Si along the different crystallographic layers the final profile is trapezoidal, with the angle determined by the etch rates. Source [http://www.cleanroom.byu.edu/KOH.phtml](http://www.cleanroom.byu.edu/KOH.phtml)
Figure 5: Surface profile for incomplete etch of oxide layer on Si. A resist layer protects the remaining oxide. A rough oxide layer is left behind due to the local variations in rate of removal of the oxide layer. Adapted from Microchip fabrication - Peter van Zant.

Figure 6: (a) A complete anisotropic etching produces vertical side walls. (b) Most often etching is partially isotropic, so that side walls are formed at an angle. Adapted from Microchip fabrication - Peter van Zant.

1.2.2 Over etch and undercutting

The opposite of incomplete etching is over etching. An ideal etchant is selective and completely anisotropic. This is essential to get vertical sidewalls when a trench is created. But, this is not always possible, so that sloped side walls are obtained, see figure 6. When the etch time is larger than the required etch time, due to isotropic etching, material under the photoresist can get removed. This is called over etching and in extreme cases it can also lead to liftoff of the resist layer, see figure 7. This is harmful, since it exposes areas of the wafer that the resist protects to the etching process.

1.2.3 Etch selectivity

Etching process should be selective to the material that has to be removed. This helps to protect the material under the mask (within limits of isotropic etching) and also the mask material itself (oxide, nitride, or resists). Consider
Si etching, using KOH. The etch rate for Si(100) at 90 °C using 30 % KOH is \( \sim 100 \mu m/hr \), see figure 2 if silicon nitride is used as mask, its etch rate, under the same conditions, is \( \sim 1 \text{nm/hr} \), nearly \( 10^5 \) times slower than Si. Thus, silicon nitride is commonly used as a mask for Si etching (especially for making Si cantilever based devices). On the other hand, silicon dioxide etch rate, under the same conditions, is \( \sim 1 \mu m/hr \), see figure 8. So, using silicon oxide as a mask will not be good enough or a very thick oxide layer is required.  

Different etchants that are used for different layers and the corresponding etch rates, shown in table 1. For Si etching, KOH is used or a mixture of nitric acid and hydrofluoric acid (HF). For silicon oxide etching, usually a mixture of HF and ammonium fluoride (NH\(_4\)F) is used, that produces a etch rate of \( \sim 0.1 \mu m/hr \) at room temperature. This mixture does not etch Si, so it provides very good selectivity. This etchant is called BOE (buffered oxide etchants). For silicon nitride, usually a strong acid like hot phosphoric acid is used at high temperatures (180 °C) since it is a very good passivating layer and hard to remove under normal conditions.

2 Dry etching

Dry etching, as the name suggest, is removal of material in the absence of solvent. The process was introduced because wet etching has some limitations in its applicability, which are listed below.

1. Wet etching is used for large pattern sizes, usually larger than 2 µm.
2. It is an isotropic process - sloped sidewalls rather than straight walls.
Figure 8: Etch rate of SiO$_2$ by KOH. Because of comparable etch rates to pure Si, it cannot be used as an etch mask for Si etching. Silicon nitride is used as the mask since its etch rate, under the same conditions, is of the order of nm/hr. Source [http://www.cleanroom.byu.edu/KOH.phtml](http://www.cleanroom.byu.edu/KOH.phtml)

Table 1: Etching chemicals used for different layers and their etch rates, under commonly used conditions. Adapted from *Microchip fabrication - Peter van Zant*.

<table>
<thead>
<tr>
<th>Material</th>
<th>Common etchant</th>
<th>Etch temperature</th>
<th>Etch rate (Å/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>HF</td>
<td>Room temperature</td>
<td>700</td>
</tr>
<tr>
<td></td>
<td>NH$_4$F (1:8)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>Acetic acid</td>
<td>Room temperature</td>
<td>1000</td>
</tr>
<tr>
<td></td>
<td>NH$_4$F (2:1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Aluminum</td>
<td>HPO$_4$</td>
<td>40-50 °C</td>
<td>2000</td>
</tr>
<tr>
<td></td>
<td>HNO (nitroxy)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Acetic acid</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>water</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
<td>H$_3$PO$_4$</td>
<td>150-180 °C</td>
<td>80</td>
</tr>
<tr>
<td>Poly Si</td>
<td>HNO$_3$</td>
<td>Room temperature</td>
<td>1000</td>
</tr>
<tr>
<td></td>
<td>H$_2$O</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>HF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
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Figure 9: (a) Starting surface after development of the resist (b) Surface after wet etching (c) Surface after dry etching. Because of the anisotropic nature of etching, dry etching produces more vertical side walls compared to wet etching, but the removal rate is slower. Adapted from Fundamentals of semiconductor manufacturing and process control - May and Spanos.

3. Wet etch has to be combined with subsequent rinse and dry steps. This increases chances of defects or contamination.

4. Hazardous chemicals and conditions are used, so safety is an issue. Safe disposal of chemicals is essential.

5. Undercutting and resist peel off can happen if time is not controlled or etch conditions change during process.

The wet and dry etching process are compared in figure 9. Dry etching is a process that overcomes some of these issues. Here, etchant gases are the primary medium for the removal of material. The basic steps involved are summarized in figure 10. There are three main types of dry etching

1. Plasma etch
2. Ion beam milling
3. Reactive ion etch

2.1 Plasma etch

In plasma etch, the chemical etchant is introduced in the gas phase. For etching silicon oxide, CF$_4$ (tetrafluoromethane) is used. The chamber is first evacuated before introducing the gas. Radio frequency (RF) electrodes are then used to generate the plasma that ionizes the gas. This ionized gas attacks the oxide layer, removing the layer. Etch rates in plasma etch are $\sim 1 - 10 \, \mu m/hr$, much smaller than wet etching. So, it more suitable for thin layers, but it also provides greater thickness control. There are different configurations for plasma etching, one such planar configuration is shown in
Figure 10: Various steps from (1) - (5) in the dry etch process. Gases are transported to the wafer surface, where they adsorb and react with the wafer surface material, at the step edges. The gases then desorb from the surface. Adapted from *Fundamentals of semiconductor manufacturing and process control* - May and Spanos.

Figure 11: Planar plasma etch configuration. The wafers are held on a grounded chuck, close to the RF electrodes. Reactive gas introduced in the chamber, is ionized and the ions helps in material removal. Adapted from *Microchip fabrication* - Peter van Zant.
Table 2: Typical plasma etching chemicals for different film materials and the corresponding gaseous products. Adapted from *Microchip fabrication* - Peter van Zant.

<table>
<thead>
<tr>
<th>Film</th>
<th>Etchant</th>
<th>Typical gas compounds</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>Chlorine</td>
<td>BCl₃, CCl₄, Cl₂, SiCl₄</td>
</tr>
<tr>
<td>Mo</td>
<td>Fluorine</td>
<td>CF₄, SF₄, SF₈</td>
</tr>
<tr>
<td>Polymers</td>
<td>Oxygen</td>
<td>DF₄, SF₄, SF₈</td>
</tr>
<tr>
<td>Si</td>
<td>Chlorine</td>
<td>BCl₃, CCl₄, Cl₂, SiCl₄</td>
</tr>
<tr>
<td></td>
<td>Fluorine</td>
<td>CF₄, SF₄, SF₆</td>
</tr>
<tr>
<td>SiO₂</td>
<td>Fluorine</td>
<td>CF₄, CHF₃, C₂F₆, C₃F₈</td>
</tr>
<tr>
<td>Ta</td>
<td>Fluorine</td>
<td>CF₄, CHF₃, C₂F₆, C₃F₈</td>
</tr>
<tr>
<td>Ti</td>
<td>Fluorine</td>
<td>CF₄, CHF₃, C₂F₆, C₃F₈</td>
</tr>
<tr>
<td>W</td>
<td>Fluorine</td>
<td>CF₄, CHF₃, C₂F₆, C₃F₈</td>
</tr>
</tbody>
</table>

**Figure II**. The resist layer used to protect the wafer is also etched along with the oxide. But the resist thickness is much larger than the oxide (few µm of resist compared to tens of nm of oxide). This means that substantial amount of resist is still available, after the etching process. Some of the different etchant gases used for plasma etching of various films are shown in table 2.

### 2.2 Ion beam etch

Ion beam etching is similar to the ion beam milling process that is used for transmission electron microscopy sample preparation. This is a physical process where ionized inert gas ions (usually Ar) are used to remove material from the wafer. The process is *not selective* but it is *highly directional*. The ion beam etching process is shown in [figure 12](#).

### 2.3 Reactive ion etching

Reactive ion etching combines the plasma and ion beam etching process to achieve both selectivity and directionality. There is an increase in selectivity compared to plasma etch, for SiO₂ and Si the selectivity ratio is 35:1 while for pure plasma etch the ratio is 10:1. This reduces the thickness requirement on the mask. Dry etch process is also used for resist stripping after patterning is complete. This is usually done by plasma etching using oxygen.
Figure 12: Schematic of the ion beam etching process. Ar gas is introduced into the vacuum chamber where they are ionized by bombarding with electrons. These ions are then directed onto the wafer where they remove material by physical bombardment. Adapted from *Microchip fabrication* - *Peter van Zant*. 
3 Deposition

The deposition process is the opposite of etching. Here, material is added to the wafer surface. The layers different from grown layers like oxide and nitride where the underlying Si is consumed during a high temperature furnace processes. In deposition, the Si from the wafer is not consumed and the wafer can be maintained at room temperature or at elevated temperatures. Some of the layers, where deposited films are used, are

1. Epitaxial layers - usually poly Si is grown for use as a gate.
2. Dielectric layers - intermetallics (high $k$ capacitors)
3. Trench capacitors
4. Intermetal conducting plugs
5. Metal layers - conductors
6. Passivation layers

Some of the deposited layers used in integrated circuits are shown in figure 13. There are two main growth techniques

1. Physical deposition
2. Chemical deposition

There are some important film parameters, which need to be controlled and these decide the type of growth technique that is adopted.

1. Thickness and uniformity
2. Roughness
3. Composition control
4. Stress
5. Purity
6. Film integrity

In most cases, the underlying substrate is not flat. The choice of technique becomes especially important when depositing in deep trenches/holes, with a high aspect ratio (depth/width) that needs to be maintained. In such cases, physical deposition techniques will not work since they will cover the hole before filling it. Physical techniques will be discussed later in the context of metallization.
3.1 Chemical vapor deposition (CVD)

There are a large number of variations to this process, but the basic principle is that chemicals containing the desired film/layer are introduced into a reactor (where the wafer is held at high temperature) in the form of a vapor. These chemicals react on the wafer surface to form the film on the wafer. Some common types of reactors for CVD process are shown in figure 14. Some examples of the chemical reactions involved in various chemical deposition processes are listed below.

\[
\begin{align*}
\text{Pyrolysis} : & \quad SiH_4 \rightarrow Si + 2H_2 \\
\text{Reduction} : & \quad SiCl_4 + 2H_2 \rightarrow Si + 4HCl \\
\text{Oxidation} : & \quad SiH_4 + O_2 \rightarrow SiO_2 + 2H_2 \\
\text{Nitridation} : & \quad 3SiH_2Cl_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2
\end{align*}
\]

(1)

CVD process can be in atmospheric conditions or under low pressure (LPCVD). LPCVD is usually used for growing silicon nitride, to reduce the comprehensive stress on the film.

For growing atomically thin films, a layer by layer growth process, called atomic layer deposition (ALD), is used. In CVD, the reacting gases are introduced into the vacuum chamber at the same time, but in ALD, the
Figure 14: Different types of CVD reactors (a) horizontal (b) pancake and (c) barrel type. The basic process in all these reactors is the same, chemicals introduced into the reactor form the final film on the wafer surface, which is held at elevated temperature. The different configurations help in control of composition uniformity and thickness. Adapted from Fundamentals of semiconductor manufacturing and process control - May and Spanos.
Figure 15: Schematic of the MBE growth chamber for GaAs. There are Ga and As sources, that are used to produce molecular beams that are deposited on the substrate and react to form the final film. Al and Si are used as dopants. The advantage of MBE is that the dopant concentration can be precisely controlled during deposition. Adapted from *Microchip fabrication* - Peter van Zant.

gases are introduced one at a time. The first gas is introduced and it forms an atomically thin adsorbed layer on the wafer. The gas is then pumped out and the second gas is introduced, which reacts with the first adsorbed atomic layer and form the final film. The second gas is then pumped out and the process repeated to grow new the new film one atomic layer at a time. The growth rate in ALD is very slow compared to CVD, but it can produce films grown layer by layer with precise control over thickness and composition.

### 3.2 Molecular beam epitaxy (MBE)

MBE is used mainly for rate control, low deposition temperature, and controlled film stoichiometry (including dopant concentration). The MBE chamber is shown in figure 15. The chamber is under ultra high vacuum ($10^{-10}$ Torr) to prevent contamination. The constituents of the film that needs to
be formed, e.g. for GaAs it would be Ga and As, are taken in their elemental or pure form in effusion cells. These are then evaporated and deposited on the substrate, where the Ga and As atoms react to form the final GaAs. Thus, molecular beams are used to form the film. If the film needs to be doped, the appropriate dopant atoms are also converted into a molecular beam and deposited along with the Ga and As, in the required concentration. By choosing the right substrate and growth conditions, epitaxial growth is also possible i.e. the lattice spacing of the film can match the substrate.

3.3 Deposited Si

Si can also be deposited on the wafer, this can either be epitaxial Si or polycrystalline Si. Poly Si is used as gate material in MOSFET provided it is heavily doped. Si is usually deposited by a CVD process, where the dopant is added along with the reactant gases. It is usually produced by a reduction process, as shown in [11] and listed below.

\[
\begin{align*}
SiCl_4 + 2H_2 & \rightarrow Si + 4HCl \\
SiH_4 & \rightarrow Si + 2H_2 \\
SiH_2Cl_2 & \rightarrow Si + 2HCl
\end{align*}
\] (2)

Depending on the wafer conditions, it is possible to get a wide variety of Si films.